FRONTGRADE Gaisler

GR740

Quad-Core LEON4FT Microprocessor Overview Presentation

October 11, 2023

FRONTGRADE Gaisler

Outline

- GR740 introduction
- Development boards and reference design
- Feature summary and architecture overview
- How to use GR740 / New features
- Key performances
- GR740 vs. UT699/UT700, GR740 vs. GR712RC
- Conclusion

Is there a later version?

Please see www.gaisler.com/GR740 for the latest version of this overview presentation

FRONTGRADE Gaisler

Outline

- **GR740 introduction**
- Development boards and reference design
- Feature summary and architecture overview
- How to use GR740 / New features
- Key performances
- GR740 vs. UT699/UT700, GR740 vs. GR712RC
- Conclusion

GR740 - Quad-core LEON4FT Processor

Value proposition

- Highest performance, wide range of interfaces
- Quad-Core LEON4: SPARC V8, Rad-hard and Fault Tolerant
- Designed as ESA's Next Generation Microprocessor, NGMP
- LEON Technology – re-use of Development and Software ecosystem
- SEU errors corrected without software interruption
- Low risk, off-the-shelf product
- QML Q/V qualified
- Excellent performance/watt ratio
    - Very low power, < 3 W (core typical)
    - Performance 1700 DMIPS (1000 MIPS)

Applications

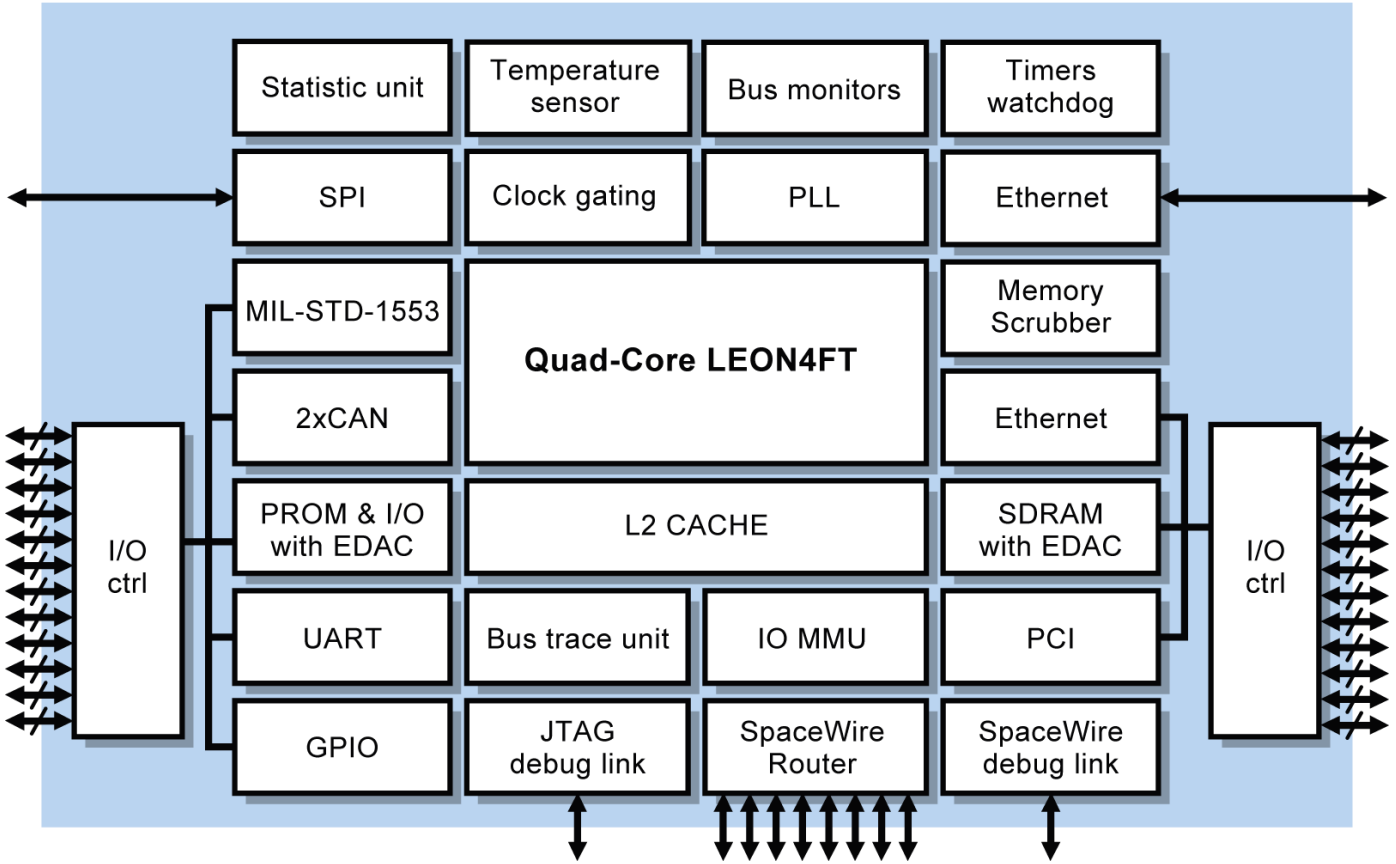
- High-performance general-purpose processing
- Symmetric and asymmetric multiprocessing
- Shared resources can be monitored to support mixed-criticality applications

For more information -> GR740 webpage

GR740 - Quad-core LEON4FT

Features

- Fault-Tolerant quad-core LEON4 processor
  - SPARC V8 integer unit with 7-stage pipeline
  - 8 register windows
  - 4x4 KiB instruction and 4x4 KiB data caches, EDAC protected
- Double-precision IEEE-754 FPU (1 FPU/Core)
- 250 MHz system frequency
- >1700 DMIPS (1000 MIPS)
- Typical core power consumption < 3W
- 2 MiB Level-2 cache
- 64-bit PC100 SDRAM memory interface with Reed-Solomon EDAC
- 8/16-bit PROM/IO interface with EDAC
- CPU and I/O memory management units
- Multi-core and multi-thread support (SMP & AMP)
- Support for time synchronisation with SpaceWire TDP controller



Interfaces

- SpaceWire router with 8 SpaceWire links (300 MHz)
- 2x 10/100/1000 Mbit Ethernet interfaces
- MIL-STD-1553B interface
- 2x CAN 2.0 controller interface
- 2x UART, SPI, Timers and watchdog, 16+22 pin GPIO
- PCI Initiator/Target interface
- JTAG

GR740 - Quad-core LEON4FT

Part no.	Processor core	Clock freq. (MHz)	Perf. (DMIPS)	TID krad (Si)	SEL LET (MeV-cm^2/mg)	Power cons.	Package	Temp. range	Qualification status	Availability	Development board
GR740 SMD: 5962-21204	Quad-Core LEON4FT	250	>1700 *	300	> 125	< 2W at 40 °C*	625-Pin Ceramic **Land** Grid Array	-40°C / +125°C (junction)	**QML Q/V**	Now	GR-CPCI-GR740 GR-VPX-GR740
GR740 SMD: 5962-21204	Quad-Core LEON4FT	250	>1700 *	300	> 125	< 2W at 40 °C*	625-Pin Ceramic **Column** Grid Array	-40°C / +125°C (junction)	**QML Q/V**	Now	
GR740 PBGA	Quad-Core LEON4FT	250	>1700 *	300	> 125	< 2W at 40 °C*	625, **PBGA**	-40°C / +105°C (case)	ESCC-Q-60-13C class 2	Now	

Complete software toolchains and debugger are available:

- Operating systems
  - RTEMS
  - WindRiver VxWorks
  - Linux 3.10+
- Simulator
  - TSIM3
- Debugger
  - GRMON3
- Qualified bootloader
  - GRBOOT

LEON

* For more information:
https://www.gaisler.com/doc/gr740/GR740-VALT-0010.pdf

FRONTGRADE Gaisler

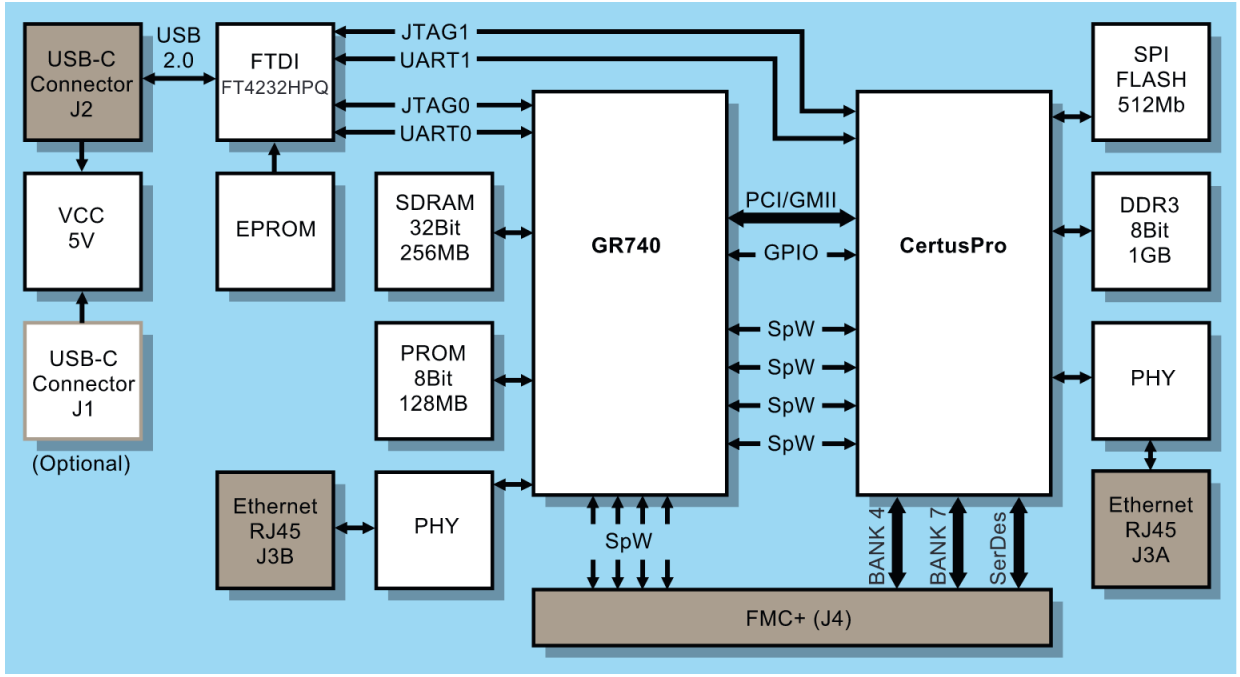
Outline

- GR740 introduction
- **Development boards and reference design**
- Feature summary and architecture overview
- How to use GR740 / New features
- Key performances
- GR740 vs. UT699/UT700, GR740 vs. GR712RC
- Conclusion

GR740-MINI Evaluation board

Evaluation Board featuring GR740PGBA & CertusPro-NX Lattice FPGA

- Small form factor (7x9.5 cm)
- USB-C connector for debug and power
- FMC+ connector
- 2x Ethernet RJ45 connectors
- Available as free-of-charge time-limited loan
- www.gaisler.com/GR740-MINI



Memory and I/O

GR740 quad-core processor

- USB-C: JTAG and UART
- 1 x Ethernet to RJ45
- FMC+: 4 x SpaceWire
- 256MB SDRAM
- 128MB FLASH

CertusPro-NX FPGA

- USB-C: UART and JTAG
- 1 x Ethernet to RJ45
- FMC+: 4 x SerDes, 23x LVDS pairs, 30 3V I/Os
- 1GB DDR3
- 512Mb SPI FLASH

GR-CPCI-GR740 Development Board

Development board designed to support development and fast prototyping of systems based on the GR740

Features

- GR740 quad-core 32-bit fault-tolerant LEON4FT SPARC V8 processor
- cPCI interface (32 bit) configurable with jumpers for Host or Peripheral operation
- PCI arbiter implemented in separate on-board FPGA
- On-board memory:
  - SDRAM SODIMM module - Delivered with two 256 MiB modules that provide a total 256 MiB of accessible data RAM plus ECC check bits
  - Parallel Boot Flash 64 Mbit (16 bit wide x 4M or 8 bit wide x 8M)
  - Additional memory via memory expansion connector
- Development Box GR-CPCI-GR740-BOX is available

GR-CPCI-GR740 Development Board

Front panel interfaces:

- Dual 10/100/1000 Ethernet interface
  - 2x RJ45
- 8x SpaceWire interfaces (8x MDM9S)
- SpaceWire debug communications link (MDM9S)
- 16-bit General purpose I/O (34 pin 0.1" ribbon cable style connector)
- FTDI Serial to USB Debug interface
  - FT4232HL with USB-Mini-AB
- LED indicators connected to GPIO signals
- DIP switch for bootstrap and PLL interface configuration
- Push button switch for reset and toggle switch (on/off) for DSU break

Interfaces at back edge of board:

- cPCI interface (32-bit), configurable for Host or Peripheral slot
- Input power connector: 5V nominal

Interfaces on-board:

- SPI interface on pin headers
- JTAG Debug interface
- 4-pin IDE style power connector
- Assorted jumpers and Test Points for configuration and test of the board

To accommodate the optional/alternative I/O interfaces the accompanying accessory board provides:

- Dual MIL-1553 Interface (Transceiver/Transformer and D-sub 9 Male connector)
- Dual CAN Interface (CAN Transceivers and two D-sub 9 Male connectors)
- Two Serial UART (RS232 transceivers and two D-sub 9 female connectors)
- SPI interface (available via 10 pin header)

GR-VPX-GR740 Development Board

Development board designed to support development and fast prototyping of systems based on the GR740

Features

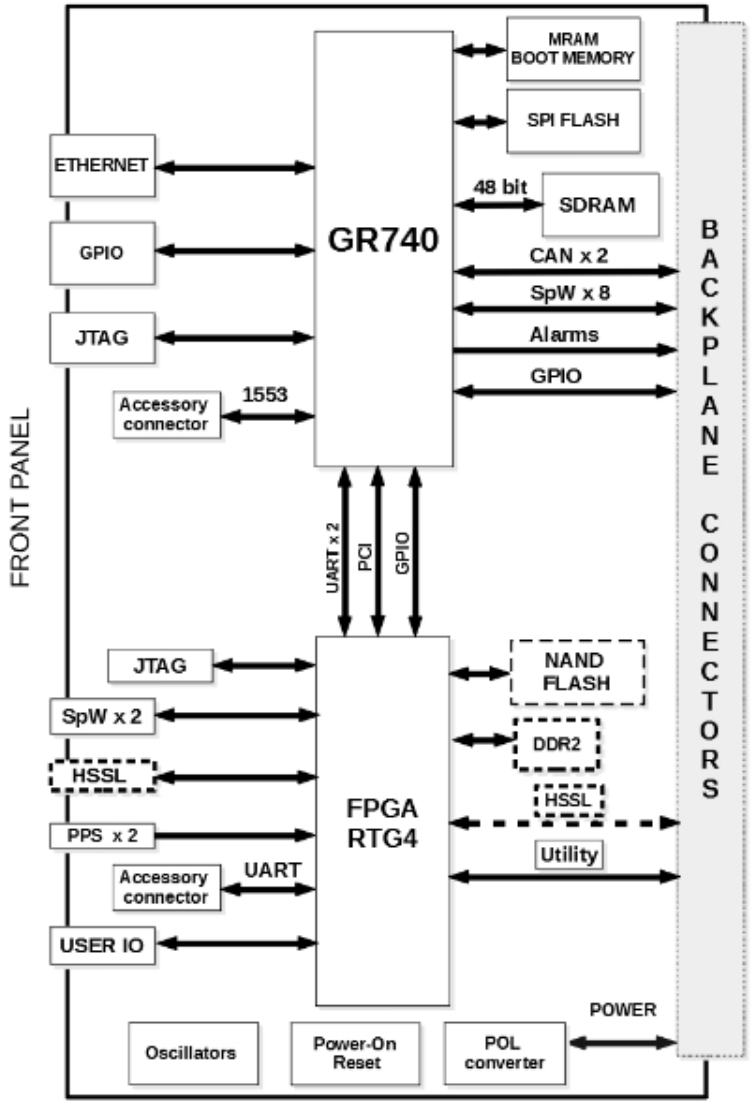
- Single board computer based on the GR740 quad-core 32-bit fault-tolerant processor
- Use in OpenVPX chassis or stand-alone
  - SpaceWire connectivity to the GR740 and to the FMC connector
- FMC connector
- On-board memory:
  - SDRAM SODIMM module - 256 MiB modules provides 128 MiB of accessible data RAM plus ECC check bits.
  - Parallel Boot MRAM 128 KiB & SPI Flash memory 32 MiB
- Front panel interfaces:
  - MIL-STD-1553B Interface (Transceiver/Transformer and D-sub 9)
  - RJ45 10/100/1000 Mbit GMII/MII Ethernet interface (KSZ9021GN)
  - 8-bit General purpose I/O (2x5 pin DIL header)
  - UART/JTAG interface using FTDI Serial-USB converter (FT4232HL/USB-uAB)
  - PPS (Pulse Per Second) input for synchronization (SMB)

- The board is provided together with an FMC mezzanine board (GR-VPX-SPW-MEZZ) which provides two SpaceWire interfaces on the front panel.

See the website for complete information

GR740 SBC Reference Design

- **GR740 SBC is a Ref Design & basic software for a single board computer based on the rad-hard GR740 Quad-Core LEON4 SPARC V8 Processor and the Microchip RTG4 radiation tolerant FPGA**
- The board developed during the ESA activity has not been qualified for flight, but a Qualification Test Plan has been established in view of a future space qualification
- **Board main features:**
  - Compact PCI Serial Space backplane connector - 6U form factor
  - Frontgrade Gaisler GR740 & Microsemi RTG4
  - SDRAM, 512 MiB + ECC check bits
  - 3D-PLUS DDR2, 512 MiB data RAM plus ECC
  - 3D-PLUS NAND FLASH, 8 GiB
  - Ethernet
  - SpaceWire:
    - 2x to front panel
    - 8x to backplane
  - High Speed Serial links to backplane
  - Redundant CAN to backplane

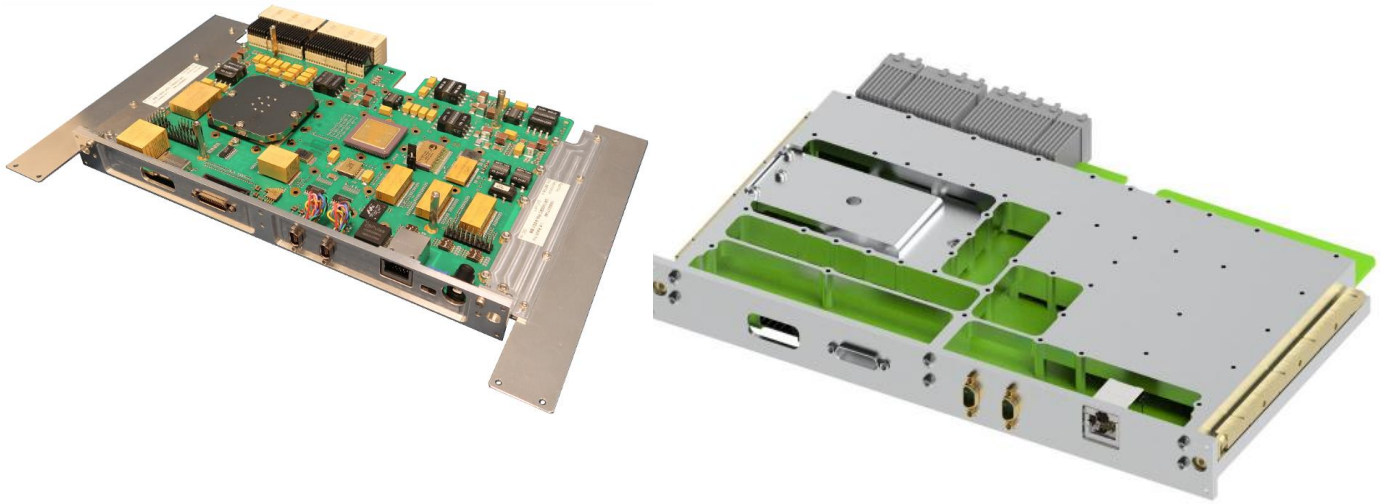


European Space Agency

GR740 SBC Reference Design Data Package

The data package consists of schematics and other design files required for developing a single board computer for flight

Design data package for Flight Model available to customers at: www.gaisler.com/gr740_sbc_refdesign



- **Hardware Detailed Design Document**
- **Board Schematics**
- **Board PCB Layout files**
- **EEE & Top Assembly BoMs**
- **Analysis reports:**
  - Worst case Analysis (WCA)
  - Board Parts Stress Analysis (PSA)
  - Radiation Tolerance
  - Thermal Analysis
  - Structural Analysis
  - Reliability Analysis
  - FMECA
- **Model descriptions:**
  - Reduced Thermal Math Model (RTMM)
  - Reduced Finite Element Method (FEM)
- **CAE files:**
  - Manufacturing files, mechanical drawings (frame, stiffeners, etc.)
  - GR740SBC power calculator
  - RTG4 FPGA Pinout details
- **User manuals:**
  - Reference Design User Manual
  - GRBOOT boot loader for GR740SBC
  - GR740SBC RTEMS drivers

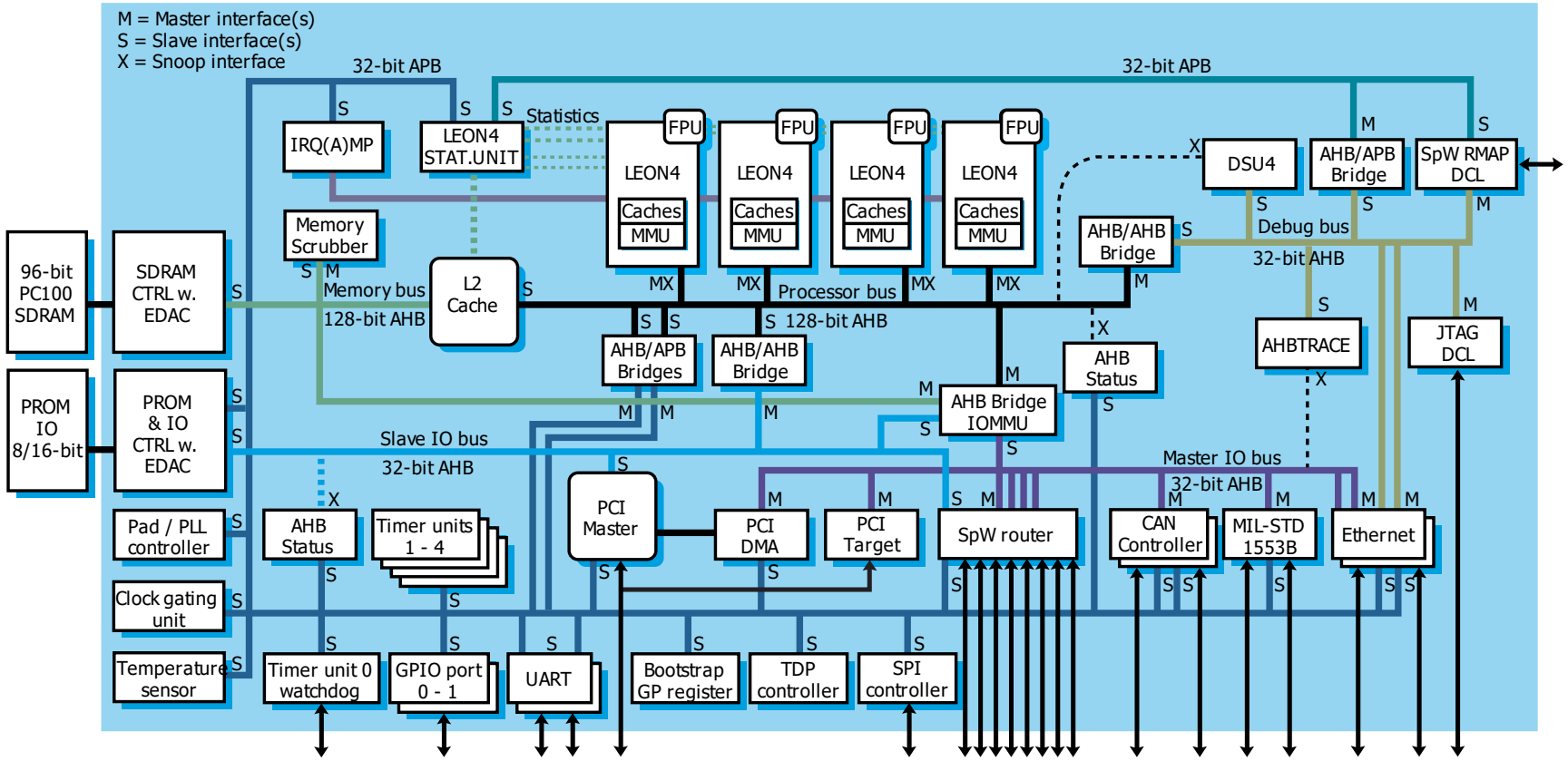
FRONTGRADE Gaisler

Outline

- GR740 introduction
- Development boards and reference design
- **Feature summary and architecture overview**
- How to use GR740 / New features
- Key performances
- GR740 vs. UT699/UT700, GR740 vs. GR712RC
- Conclusion

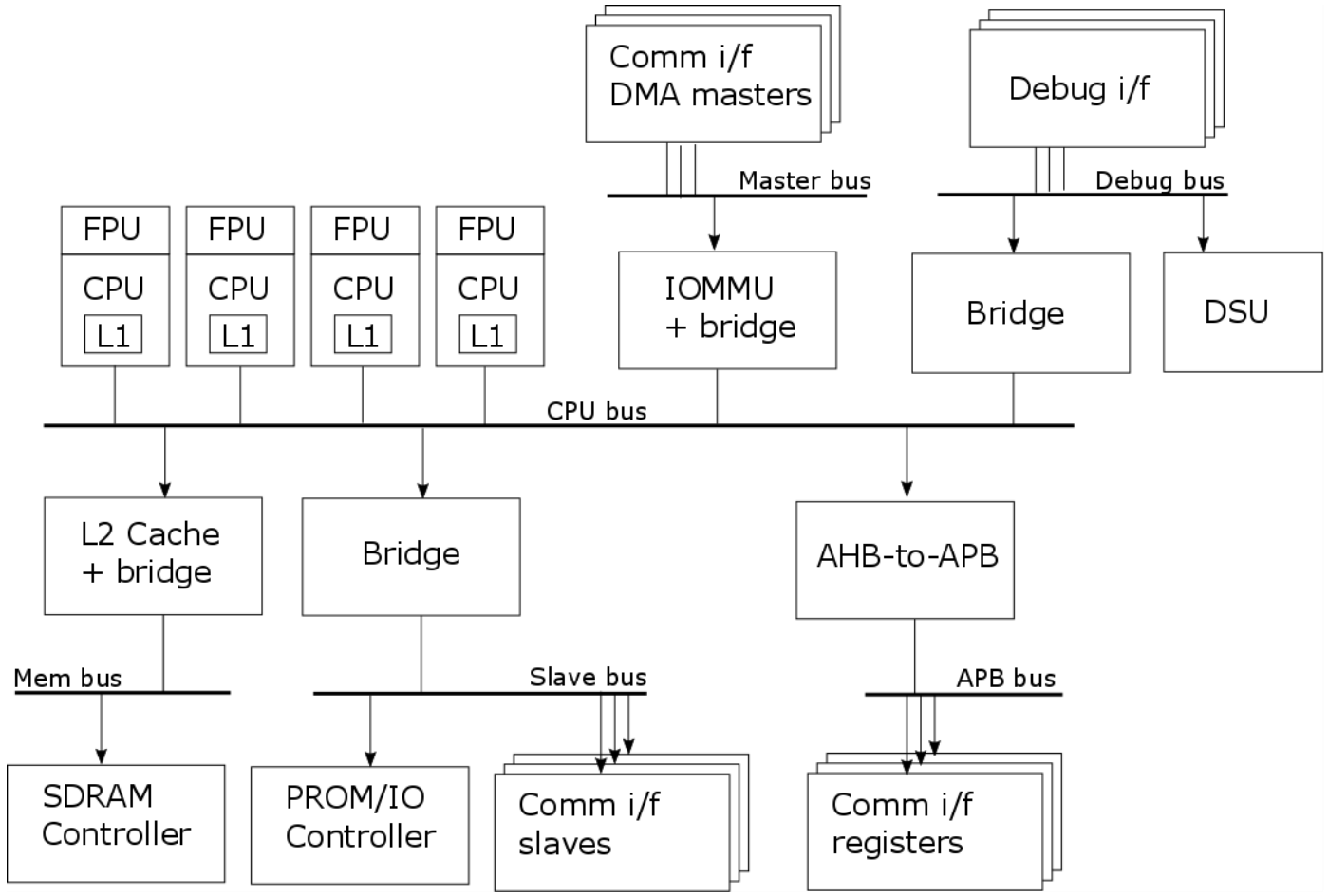
Feature Summary – Core components

- 4x LEON4 fault-tolerant CPUs with L1 cache, MMU and FPU
- 2 MiB Level-2 cache
- 96/48-bit SDRAM controller with EDAC and scrubber
- 8/16-bit PROM/IO controller with EDAC in 8-bit mode
- 5x Timer, 5x IRQ controller
- On-chip AHB bus infrastructure
- IOMMU for peripheral DMA
- PLLs for clock generation
- Communication interfaces



Feature Summary – Block diagram

- Simplified architecture block diagram



Feature Summary – Interfaces

- Interfaces
  - 8-port SpaceWire router with on-chip LVDS
  - 2x 1000/100/10 Mbit Ethernet MAC (GMII/MII)
  - PCI master/target with DMA, 33 MHz
  - MIL-STD-1553B interface (bus A/B)
  - 2x UART
  - 16x GPIO

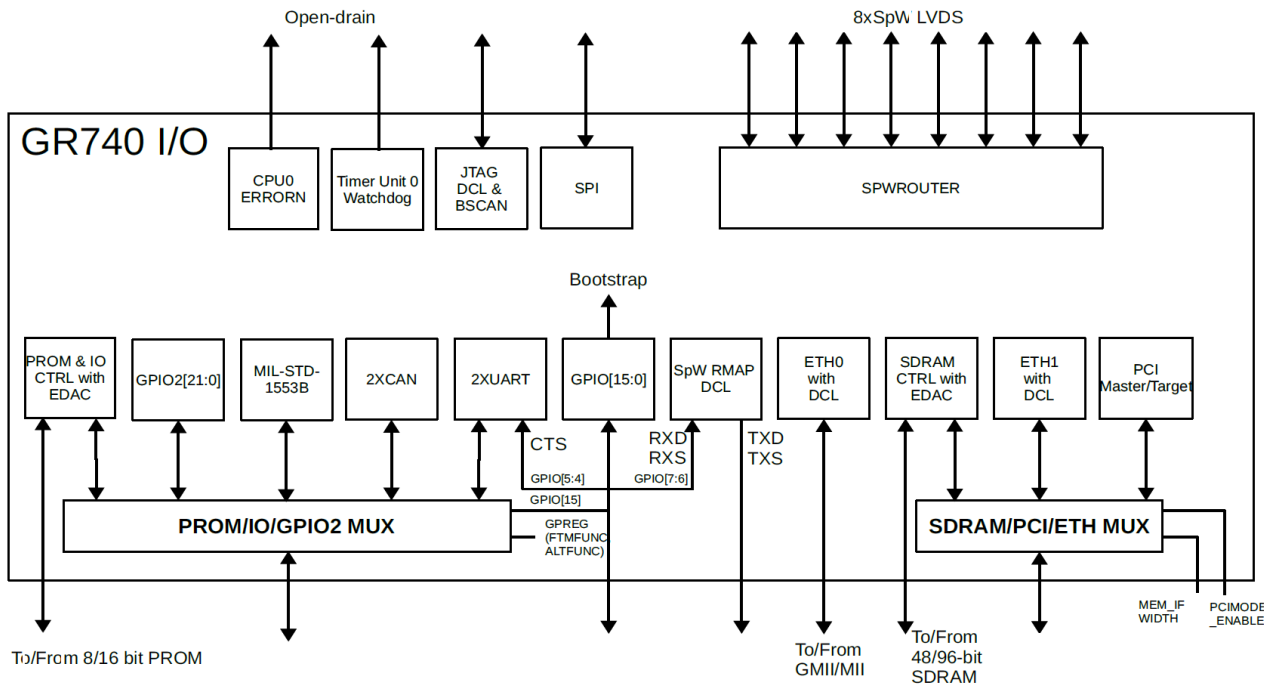
- Debug interfaces (for GRMON3 connection)
  - Ethernet EDCL (using either of the two MACs)
  - JTAG
  - SpaceWire RMAP (using separate GRSPW2 controller for debug only)

Feature Summary – Interface restrictions

- Some functions are multiplexed onto the same pins
- Either PCI or second Ethernet (not both) can be enabled only when SDRAM is in 48-bit mode
  - Configured “hard” via bootstrap signals
  - Selection of

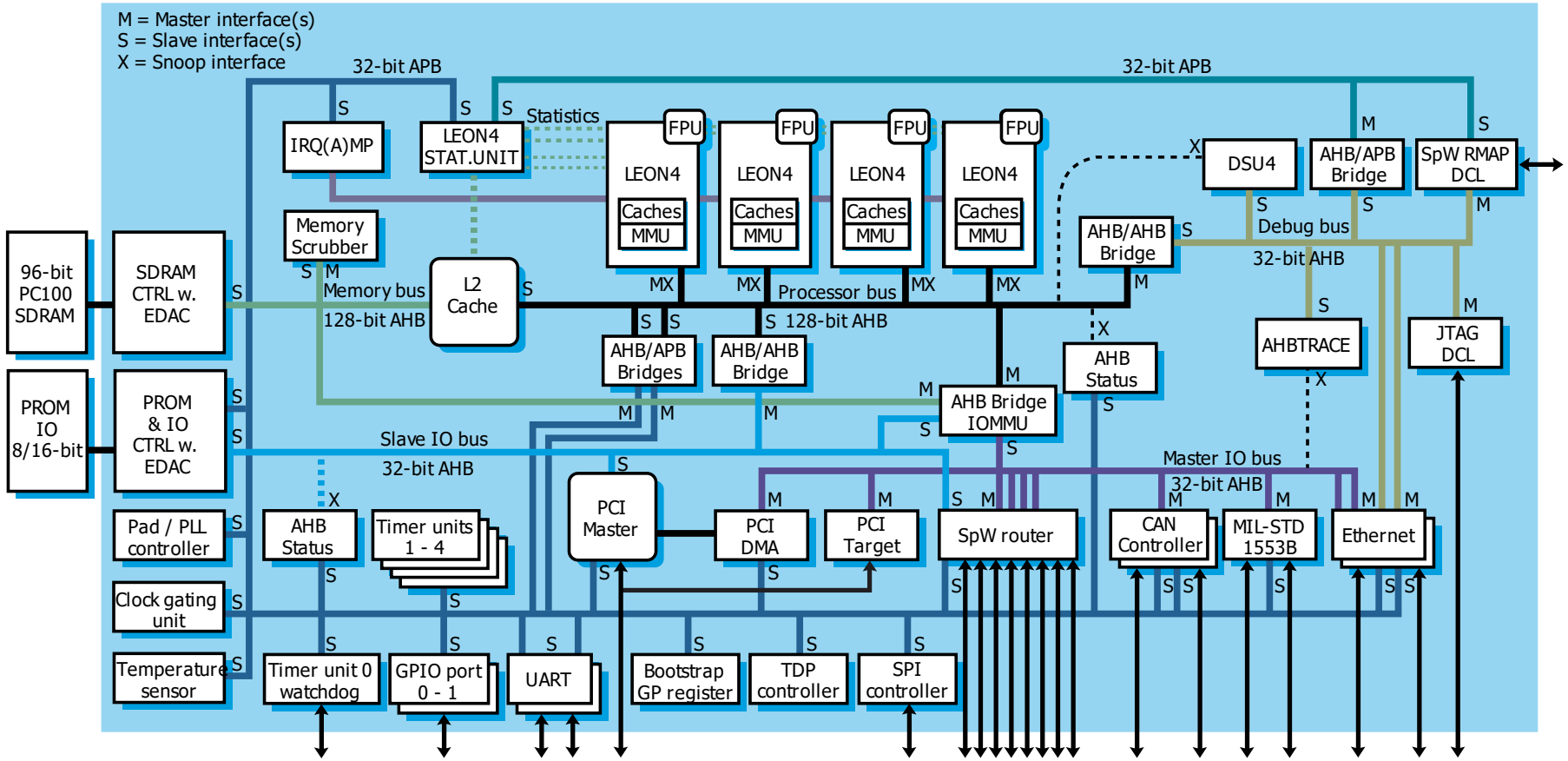
  (1) 96-bit SDRAM + 1x ETH
  (2) 48-bit SDRAM + 2x ETH
  (3) 48-bit SDRAM + 1x ETH + PCI

- CAN, MIL-STD-1553B, UART, and SpaceWire debug are shared with PROM top address bits and part of 16-bit PROM data bus (unused in 8-bit mode).
  - Configurable pin-by-pin between PROM and peripheral function
  - Pins that are not used for either function can be used as additional GPIO



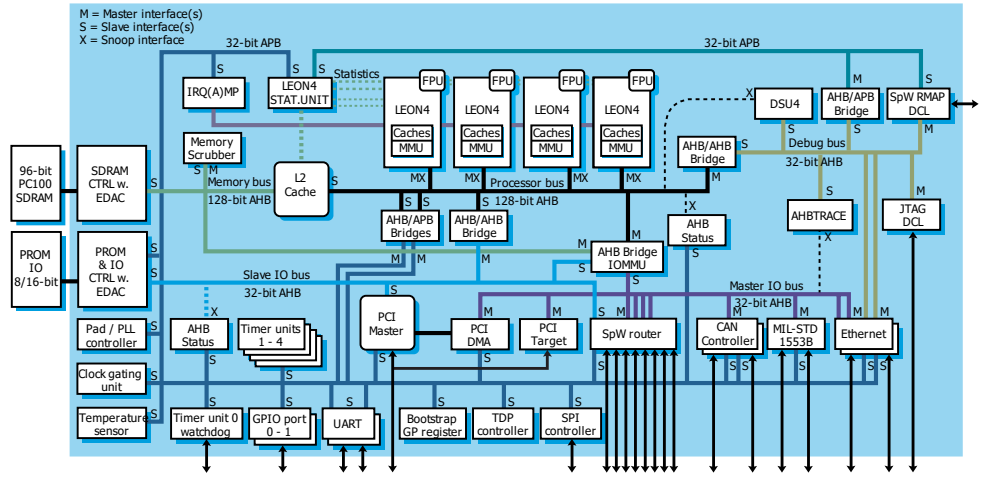
GR740 Overview – Block diagram

- Bus topology with five AMBA AHB buses: Processor, Memory, Master IO, Slave IO, and Debug. Low-speed peripherals via APB.
- Debug AHB bus and corresponding peripherals are gated off (no clock, disconnected by multiplexers) in flight.



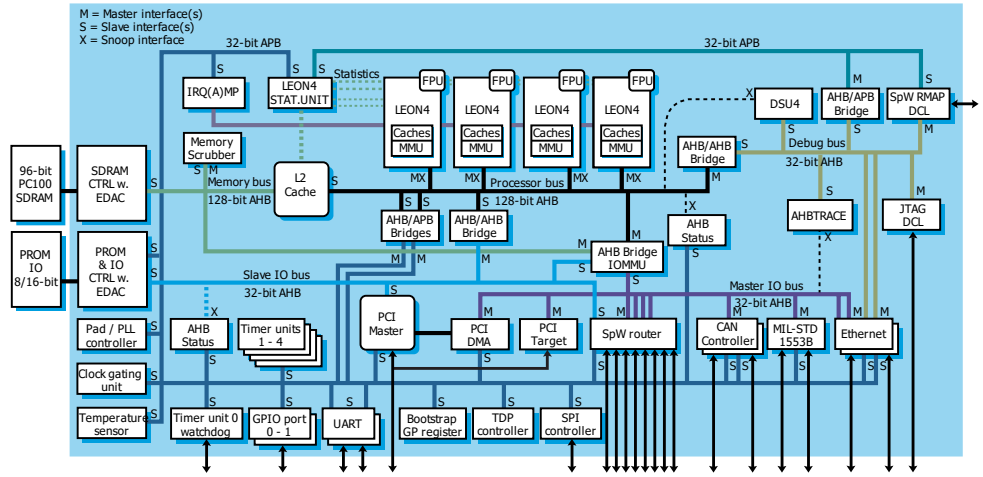
GR740 Overview – LEON4FT and GRFPU

- LEON4FT – IEEE1754 SPARC V8 compliant 32-bit processor
  - 7-stage in-order pipeline, multiprocessor support
  - 128-bit AHB bus interface
  - Compare-and-Swap (CASA) instruction support (from SPARCv9)
- GRFPU
  - High-performance FPU integrated into LEON4 pipeline
  - Hardware DIV and SQRT
  - Floating-point controller (FPC) decouples FP operations from pipeline, allowing CPU and FPU to work in parallel.



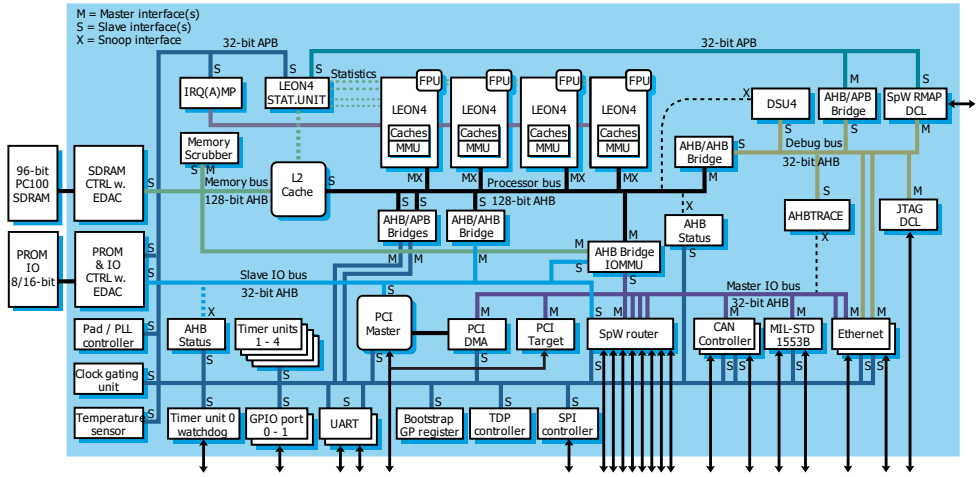
GR740 Overview – Caches

- Level-1 cache
  - Separate L1 integrated into each LEON4 core
  - Multi-set with configurable LRU/LRR/RND policy
  - Write-through operation
  - Bus snooping with physical tags to maintain coherency
- Level-2 cache
  - Designed as a bridge in the bus topology
  - Highly configurable in caching behaviour
  - Supports copy-back operation
  - Locked ways, allowing part or whole to be used as on-chip RAM
  - Can be partitioned based on bus master indexes



GR740 Overview – Memory subsystem

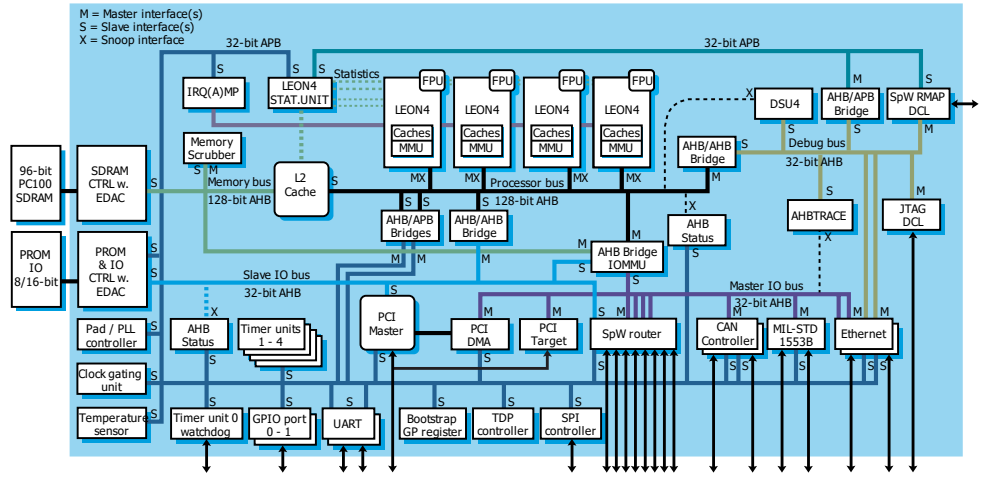
- Memory controller
  - SDRAM with 64/32 data bits and 32/16 check bits
  - Full width or half-word selected via bootstrap signals
  - Powerful interleaved 16/32+8bit ECC giving 32 or 16 checkbits
- Scrubber
  - Fast initialization of memory and checkbits
  - Background scrubbing
  - Error reporting to CPU and statistics collection
- Memory error handling (memory controller, scrubber, CPU)
  - Rapid regeneration of contents after SEFI
  - Graceful degradation of failed byte lane
  - Example code available for RTEMS
  - Boot memory provided via PROM/IO interface (same controller as UT699, GR712RC)



GR740 Overview – I/O interfaces

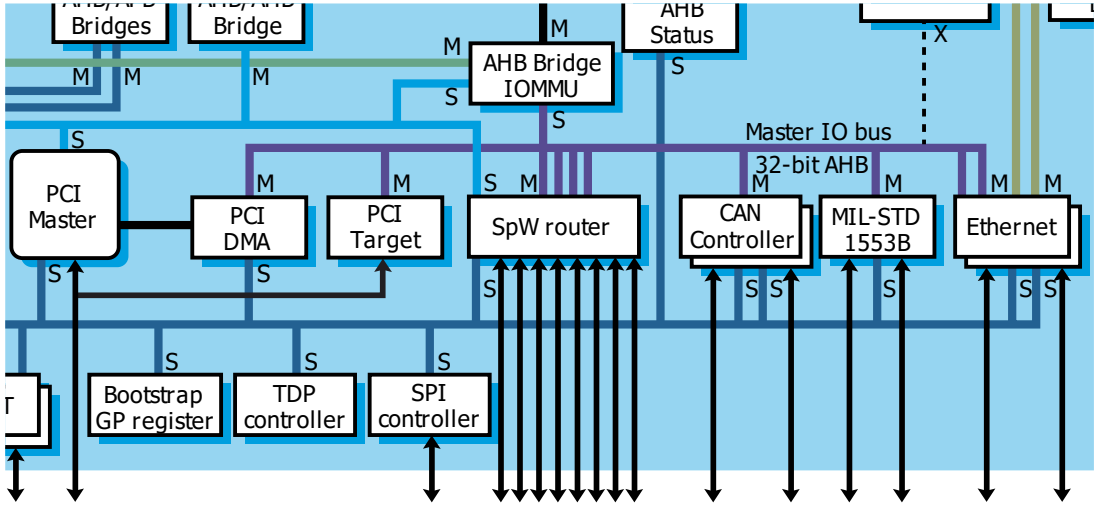
- Large number of I/O interfaces
  - SpaceWire router
  - PCI master/target with DMA
  - Gbit Ethernet
  - MIL-STD-1553B
  - CAN 2.0B
  - UART, SPI, GPIO

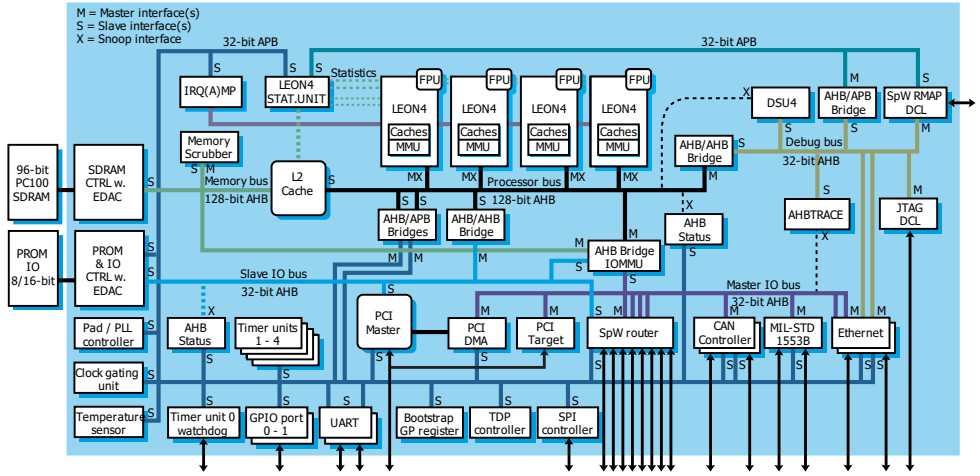
- Debug interfaces
  - Ethernet
  - SpaceWire (RMAP)
  - JTAG



GR740 Overview – I/O interfaces connected through IOMMU

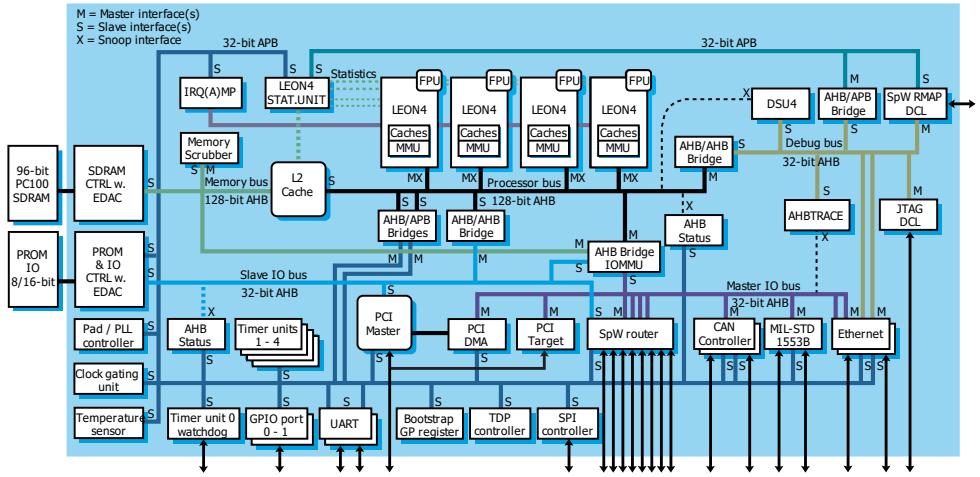
- IOMMU
  - Connects all DMA capable I/O masters through one interface to the Processor bus
  - Performs pre-fetching and read/write combining
  - Provides address translation and access restriction
  - Uses separate page tables from processor
  - Masters can be placed in groups where each group has its own set of page tables
  - Master traffic can also be routed directly to Memory bus, bypassing Level-2 cache





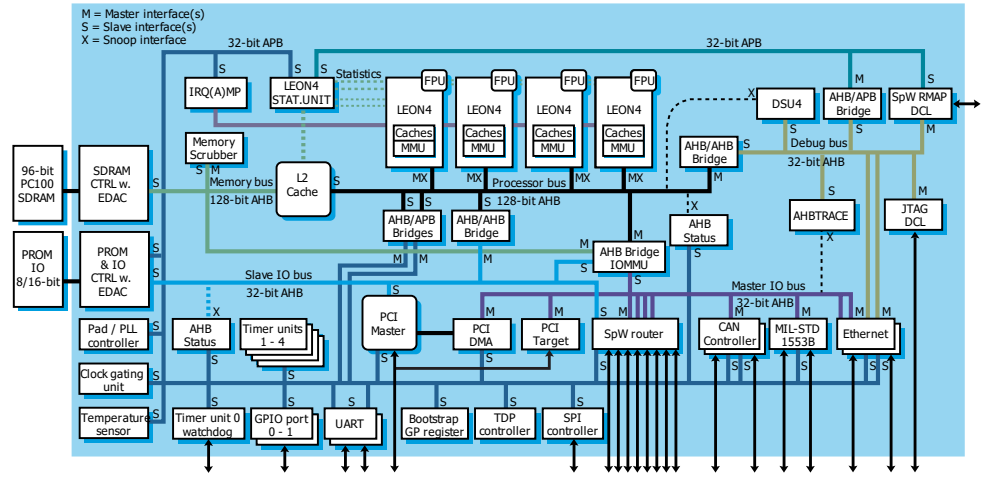
GR740 Overview – SpaceWire router

- SpaceWire router
  - Four internal AMBA ports with DMA support, compatible with GRSPW2.
  - Eight external SpaceWire ports
  - One configuration port with RMAP target support which can be used for remote access to the system.
  - Feature support for
    - Group adaptive routing
    - Packet distribution
    - System time-distribution
    - Distributed interrupts
    - Deadlock recovery
    - SpaceWire-D packet truncation
    - SpaceWire Plug-and-Play
  - Register configuration allows to turn off unused LVDS drivers on SpaceWire links for power saving.
  - Same IP core as used in GR718B SpaceWire router standard product
  - SpaceWire link speed: up to 300 Mbit/s



GR740 Overview – PCI master (initiator) / target with DMA

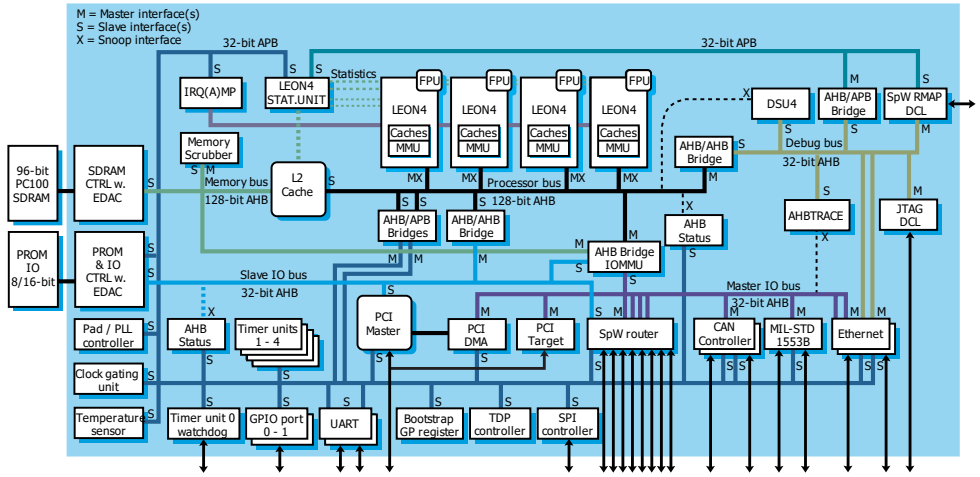
- Provides PCI master/target interface
  - Provided by GRPCI2 core (vs. GRPCI for UT699/UT699E/UT700)
  - 32-bit interface supporting 33 MHz operation
  - Not fully compliant to PCI 2.3 due to lack of suitable pads and pin multiplexing.
  - Target has three configurable PCI BARs. BAR0 and BAR1 default to prefetchable 128 MiB BARs and BAR2 defaults to a non-prefetchable 8 MiB BAR.
  - Pins shared with SDRAM interface: If PCI is enabled then the data width of the SDRAM interface is reduced to 32-bits. Pins are also shared with second Gigabit Ethernet interface.



GR740 Overview – Gigabit Ethernet

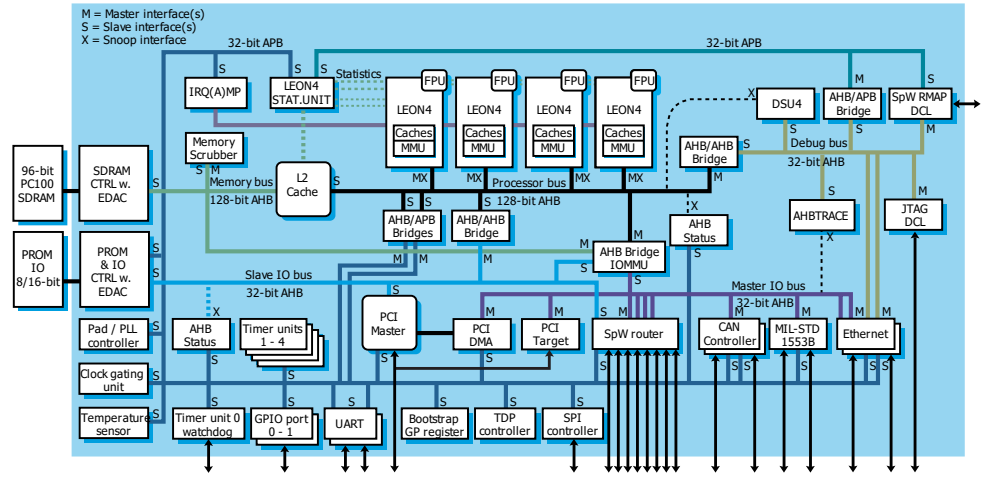
- Gigabit Ethernet interfaces
  - 2x Ethernet interfaces
  - Supports 10/100/1000 Mbit in both full- and half-duplex
  - DMA engine for both receiver and transmitter
  - Internal buffer allows core to buffer complete packet
  - Supports MII and GMII interface to external transceiver
  - Supports scatter/gather IO and IPv4 checksum offloading
  - Provides Ethernet Debug communication link
  - EDCL can also be connected to Debug bus

- Pins of second Ethernet interface are shared with SDRAM interface: If second Ethernet interface is used then the data width of the SDRAM interface is reduced to 32-bits. Pins are also shared with PCI interface (second Ethernet interface only).



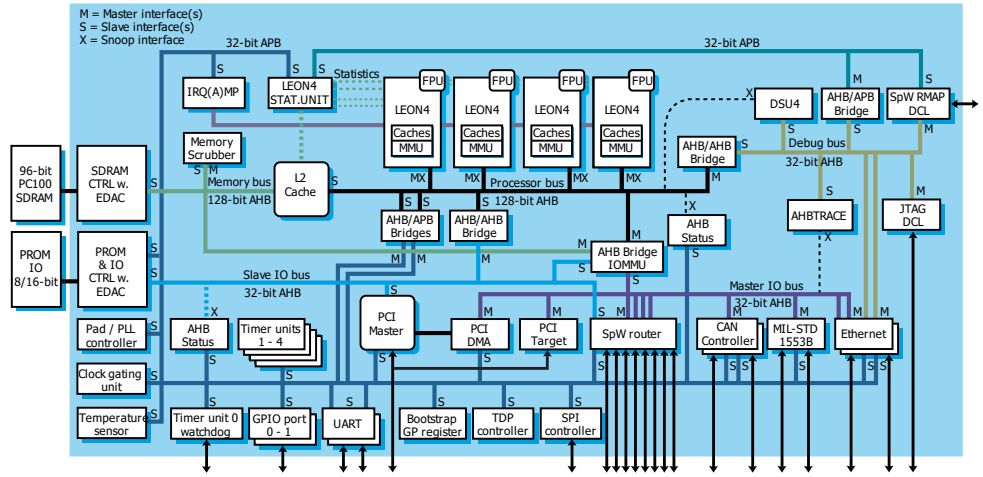
GR740 Overview – CAN 2.0B

- CAN 2.0B controller with internal DMA engine
  - Two CAN controllers connected to same two CAN buses. Redundancy implemented by Selective Bus Access.
  - AHB master interface performs burst DMA accesses between the memory and CAN controllers, when Tx/RX transfers are set up via APB registers.
  - Separate buffers for transmission and reception.
  - Nominal and redundant transmit input and receive output. Configurable via APB registers
  - Supports synchronization message detection and interrupt generation.
  - Interrupt generation on different events like transmission, reception, communication errors etc.
  - Detailed CAN interface status monitoring support.



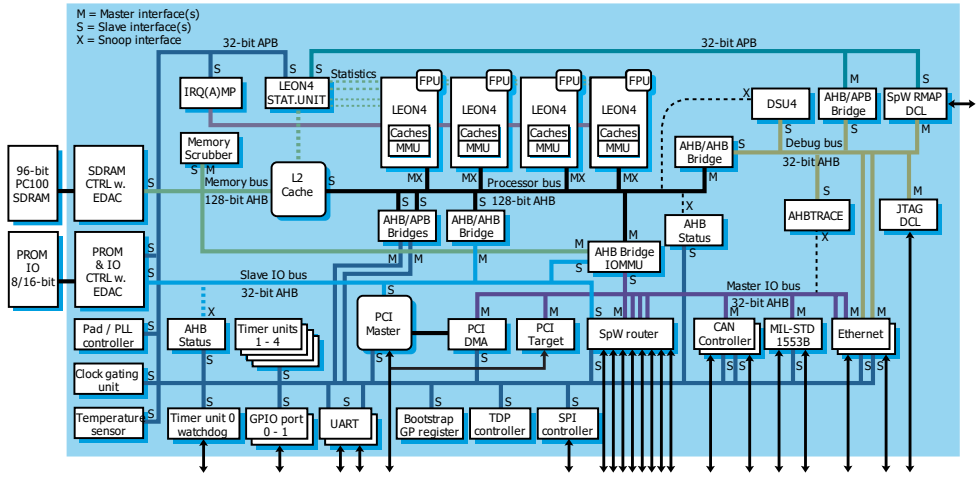
GR740 Overview – MIL-STD-1553B, UART, SPI, GPIO

- MIL-STD-1553B controller provided BM/BC/RT functionality with dual redundant buses.
  - Has internal DMA engine.
- Two 8-bit UARTs with 16-byte FIFOs
- SPI master/slave controller
  - Configurable word length (3-32 words)
- Two general purpose I/O ports



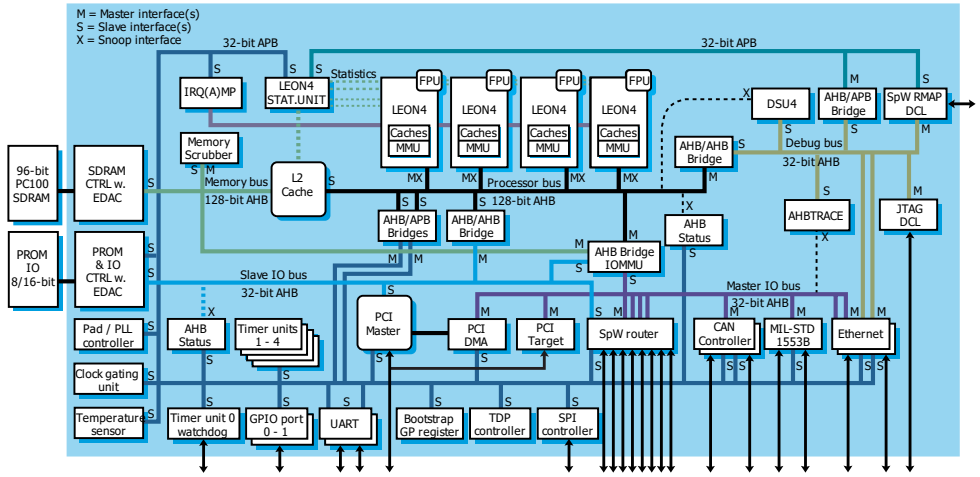
GR740 Overview – Debug interfaces and Debug bus

- Debug bus
  - Debug support unit
  - PCI trace buffer
  - AHB trace buffer, monitoring Master IO bus
  - APB bridge allows direct access to performance counters
- Debug links
  - JTAG Debug Communication Link
    - Bandwidth: 500 kb/s
- SpaceWire RMAP target
  - Bandwidth 20 Mb/s
- Ethernet Debug links
  - Bandwidth: >100 Mb/s
  - Can optionally be connected to Master IO bus



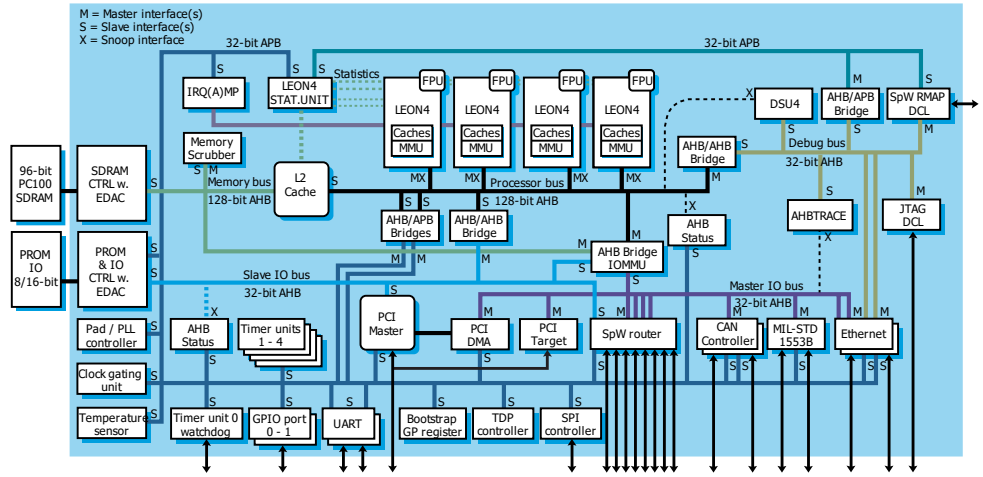
GR740 Overview – Improved debug support

- Debug support improved compared to earlier LEON devices
  - High-speed debug interfaces
  - Non-intrusive debugging through dedicated Debug bus
  - AHB trace buffer with filtering
  - Instruction trace buffer with filtering – can be read during execution
  - Hardware data watchpoints, Data area monitoring
- Improved profiling support – with support for filtering
  - I/D cache/TLB miss/hold
  - Data write buffer hold, Branch prediction miss
  - Total/Integer/FP instruction count
  - Total execution count
  - L2 accesses, misses
  - AHB bus statistics



GR740 Overview – Resource partitioning

- Resource partitioning allows running separated software instances
  - The architecture has been designed to support both SMP, AMP and mixtures (example: 3 CPU:s running Linux or VxWorks SMP and one running RTEMS)
  - The L2 cache can be set to 1 way/CPU mode. Cache has fence registers that can be used to protect software.
  - IRQs can be masked/routed separately to each CPU
  - The I/O peripherals' register interface are located at separate 4k pages to allow (via MMU) restricting user-level software from accessing the "wrong" peripheral
  - IOMMU allows placing DMA peripherals into groups and offers modes with protection and address translation



FRONTGRADE Gaisler

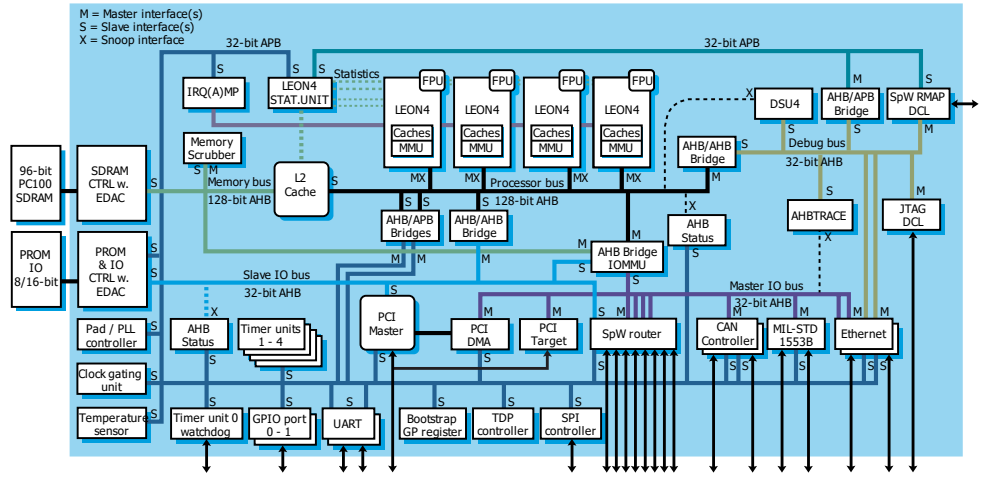
Outline

- GR740 introduction
- Development boards and reference design
- Feature summary and architecture overview
- **How to use GR740 / New features**
- Key performances
- GR740 vs. UT699/UT700, GR740 vs. GR712RC
- Conclusion

How to use GR740 – Taking advantage of the four LEON4FT

- Advantage: More processing power, more functions on one chip
  - Design goal of maximum average performance has a cost in jitter/predictability
  - Linux/VxWorks/RTEMS has SMP support.

- UP instances of RTEMS/VxWorks/Bare-C/Other can be used by linking images to separate memory areas
  - Booting multiple images is supported by MKPROM2
  - May need static MMU tables to enforce (space) separation
  - Developer needs to assign HW resources
  - Apart from added set up work, no news
    - More functions on one chip
    - Cost is added timing jitter



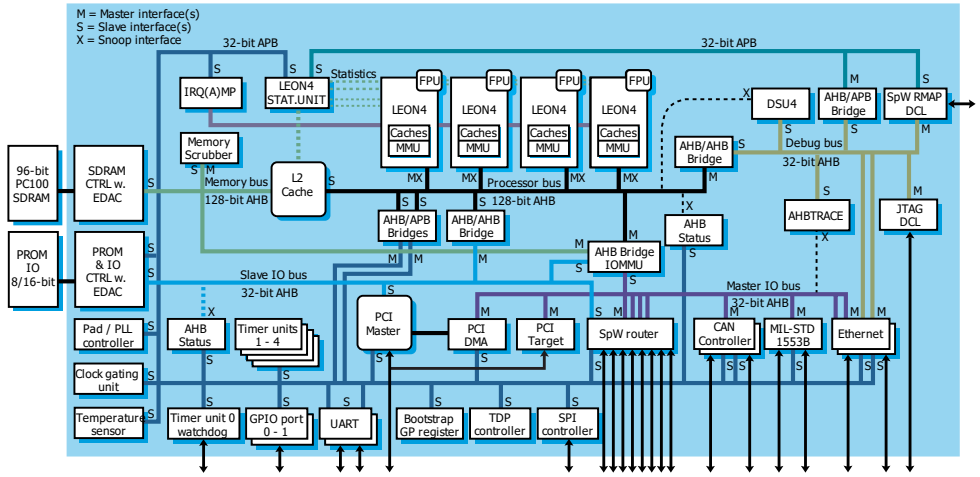
How to use GR740 – PROM-less / SpW applications

- PROM-less booting possible via SpaceWire
  - Connect via RMAP
  - Configure main memory controller
  - Use HW memory scrubber to initialize memory
  - Enable L2 cache
  - Upload software
  - Assign processor start address(es)
  - Start processor(s)
- SpaceWire router, with eight external ports, is fully functional without processor intervention.

- Device can also act as a software/processor-free bridge between SpaceWire and PCI/SPI/1553 etc.

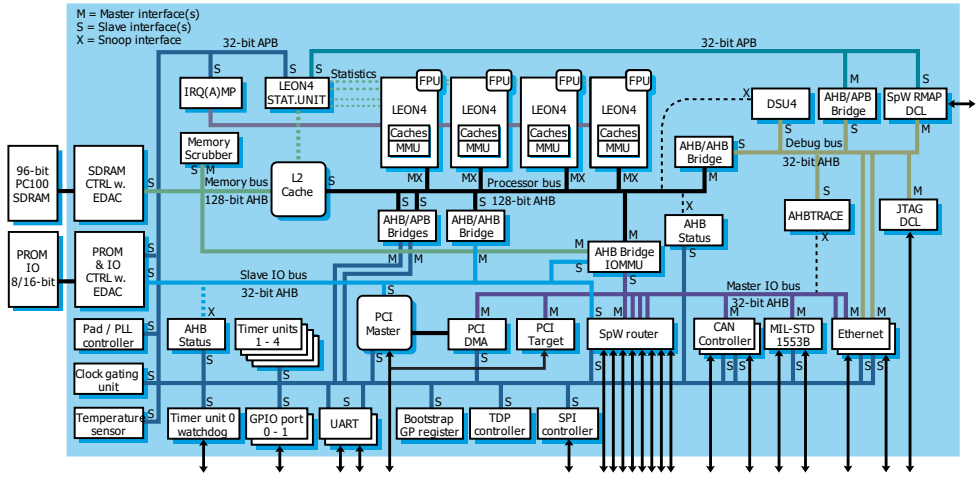
- IOMMU can be used to restrict RMAP access.

- Application note GRLIB-AN-0002 *Booting a LEON system over SpaceWire RMAP* @ www.gaisler.com/notes



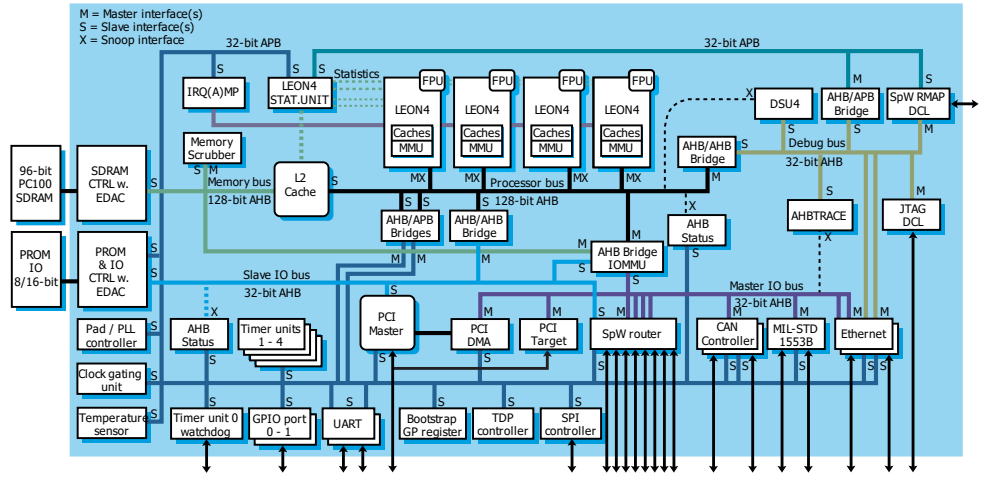
How to use GR740 – Clock gating

- Clock gating is controlled via clock gating unit
  - Automatic clock gating of processor cores that are in idle mode
  - Separate gating of floating-point units. FPU is gated-off when it is disabled.
  - Clock gating unit also controls clock and reset for the following peripherals:
    - Ethernet controllers
    - SpaceWire router
    - PCI target/initiator with DMA unit
    - MIL-STD-1553B controller
    - CAN 2.0B controller
    - UARTs
    - SPI controller
    - PROM/IO memory controller
- Debug bus is gated-off when DSU is disabled.



GR740 New Features – (Some of them)

- Features in GR740 not found in previous LEON/LEON-MP architectures:
  - Quad-core LEON4FT
  - L2 cache with locking
  - Wide AMBA buses
  - Improved support for partitioning
    - IOMMU
    - Per-processor timers and interrupt controllers
  - Improved debug support (#links, filters, performance counters)
  - Improved support for AMP (address mapping, number of cores)
  - Boot options (PROM, RMAP, PCI)
  - Hardware memory scrubber



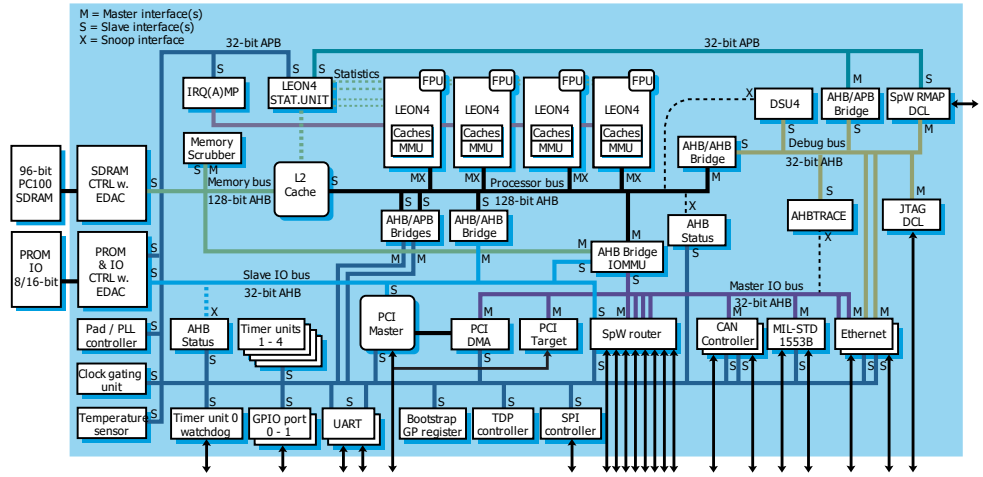
FRONTGRADE Gaisler

Outline

- GR740 introduction
- Development boards and reference design
- Feature summary and architecture overview
- How to use GR740 / New features
- **Key performances**
- GR740 vs. UT699/UT700, GR740 vs. GR712RC
- Conclusion

Key Performances

- System clock (CPU:s, L2Cache, on-chip buses)
  - Nominal frequency is 250 MHz, generated by PLL from external 50 MHz clock (STA and prod. test)
  - Full temp range (-40 to +125 Tj) with margins for aging and clock jitter
  - 4 CPUs x 250 MHz x 1.7 DMIPS/MHz = 1700 DMIPS
- Memory clock
  - 100 MHz supported internally and achieved on evaluation board (using commercial SDRAMs and external clock buffer).
  - Achievable clock frequency on space-grade board depends on I/O timing and clocking scheme.
  - Some mitigation techniques have been implemented to support high-load scenarios (2T command signaling, duplicated CS# lines)



FRONTGRADE Gaisler

Outline

- GR740 introduction
- Development boards and reference design
- Feature summary and architecture overview
- How to use GR740 / New features
- Key performances
- **GR740 vs. UT699/UT700, GR740 vs. GR712RC**
- Conclusion

Processor comparison

Part Number	UT699	UT699E	UT700	GR712RC	GR740
Processor	LEON3FT Single Core 32-bit SPARC V8	LEON3FT Single Core 32-bit SPARC V8	LEON3FT Single Core 32-bit SPARC V8	LEON3FT Dual Core 32-bit SPARC V8	LEON4FT Quad Core 32-bit SPARC V8
Foundry	TSMC (250nm)	TSMC (130nm)	TSMC (130nm)	TowerJazz (180nm)	ST (65nm)
Operating Voltage (core/IO)	2.5V/3.3V	1.2V/3.3V	1.2V/3.3V	1.8V/3.3V	1.2V/2.5&3.3V
Clock Frequency	66 MHz	100 MHz	166 MHz	100 MHz	250 MHz
DMIPS/Core, total	92	140	230	140, 280	425, 1700
Cache L1 I/D (KiB)	8/8	16/16	16/16	16/16	16/16
Cache L2 / L3 (KiB)	No	No	No	No	2048KB
MMU	Yes	Yes	Yes	Yes	Yes
SpaceWire	2 x DMA 2 x DMA/ RMAP	4 x DMA/ RMAP	4 x DMA/ RMAP	2 x DMA/ RMAP Up to 4 x 200 Mb/s DMA	8 x 300 Mb/s DMA/ RMAP
Ethernet	No	No	No	10/100	10/100/1000
CAN	2	2	2	2	2
1553	No	No	1	1	1
SPI	No	No	Yes	No	Yes
PCI	Yes	Yes	Yes	No	Yes
Other interfaces					

GR740 vs UT699/UT699E/UT700

- LEON4 in GR740 improves performance (1.7 DMIPS/MHz vs. 1.4 DMIPS/MHz).
- Maximum frequency increase: 250 MHz for GR740
- Quad-processor system provides additional performance improvement. Up to a speed-up of four but in reality lower due to shared bus and SW synchronization requirements.
- UT* has 10/100 Mbit Ethernet. GR740 has 10/100/1000 Mbit.
- UT699/UT699E lacks MIL-STD-1553B. Present in GR740 and UT700.
- GR740 provides four AMBA ports and eight SpaceWire ports with a router. UT* has four SpaceWire interfaces.

GR740 vs GR712RC

- LEON4 performance improvement over LEON3FT
- CCGA vs CQFP package
- Reduced power consumption
- 250 MHz GR740 vs 100 MHz GR712RC
- Quad-core system with Level-2 cache vs. dual-core system with shared memory controller.
- Level-2 cache reduces impact of shared memory.
- GR712RC has shared resources for memory controller, timer unit. GR740 improves HW support for partitioning by mapping addresses on 4k boundaries and including additional HW units.
- Timing / interference analysis possible for dual-core GR712RC system as demonstrated by CNES. Shared L2 cache more difficult to analyze but this is mitigated by inclusion of performance counters to count accesses to shared resources and L2 partitioning.

FRONTGRADE Gaisler

Outline

- GR740 introduction
- Development boards and reference design
- Feature summary and architecture overview
- How to use GR740 / New features
- Key performances
- GR740 vs. UT699/UT700, GR740 vs. GR712RC
- **Conclusion**

Conclusion

- GR740 is immediately available and support by Frontgrade software packages and development tools
- Latest information available at www.gaisler.com/GR740