GR-CPCI-XC7K Development Board

User Manual

COBHAM GAISLER AB
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Cobham Gaisler AB
Kungsgatan 12
411 19 Göteborg
Sweden

tel +46 31 7758650
fax +46 31 421407
sales@gaisler.com
www.gaisler.com

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REVISION HISTORY

Revision	Date	Page	Description
0.0 DRAFT	2015-04-15	All	Draft
1.0	2015-11-05	All	First issue after manufacturing of prototypes

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1 INTRODUCTION

1.1 Overview

This document describes the *GR-CPCI-XC7K* Development Board.

The purpose of this equipment is to provide developers with a convenient hardware platform for the evaluation and development of software for *Cobham Gaisler GRLIB/LEON* designs.

The *GR-CPCI-XC7K* Development Board comprises a custom designed PCB in a 6U Compact PCI format, making the board suitable for stand-alone bench top development, or if required, to be mounted in a 6U CPCI Rack.

The main element of this design is a *Xilinx Kintex XC7K325T* FPGA making the functions of this board both re-programmable and flexible.

The principle interfaces and functions are accessible on the front and back edges of the board, and secondary interfaces via headers on the board.

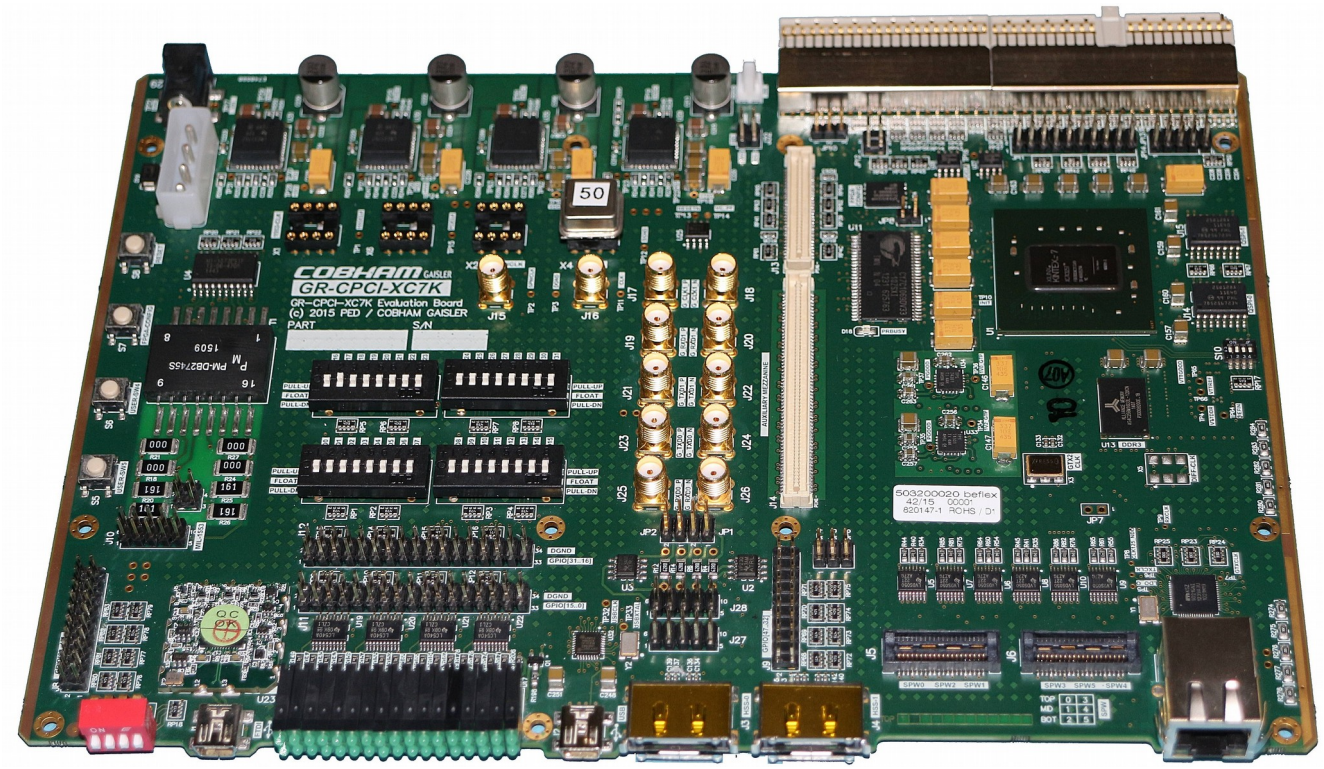

Figure 1-1: GR-CPCI-XC7K Development Board

The board contains the following main items as detailed in section 2 of this document:

- Xilinx Kintex7 XC7K325T900 FPGA
- Gbit Ethernet with (G)MII interface to FPGA and RJ45 connector on front panel
- Six SPW (LVDS) interfaces with on-board LVDS transceivers and front-panel MDM9S connectors
- Two CAN interfaces with on-board CAN transceivers and headers which connector to front-panel MDM9 connectors
- USB2.0 interface with ULPI connection to the FPGA and with USB-MINI-AB connector on front panel
- Two E-SATA front panel connectors connected to the Xilinx GTX high-speed serial transceiver interfaces for the FPGA, for SRIO interfaces
- Dual MIL-1553 interface with front panel DSUB 9 Male connector
- 32 General Purpose I/O signals on headers which are connected to the front panel
- Octal SPDT DIP Switches for configurable Pull-up/Pull-down of the GPIO pins to allow a configurable power-on pin-strapping to be implemented
- 32 front panel LED's indicating the high/low state of the multi-function GPIO pins
- Additional 32 General Purpose I/O signals on two 20 pin headers, compatible with ribbon cable connections with *GR-Accessory* boards (e.g. RS232 UART)
- 2 front panel LED's indicating the '*POWER*' and '*FPGA DONE*' status
- A push button for *RESET* and for a User defined function (nominally *DSU Break*)
- Four DIP switches accessible from the front panel for User Defined functions
- JTAG Programming interface with on board programming circuit and front panel USB-Mini-AB connector
- Compact PCI connector to with 32 bit PCI interface with 4 channel Arbiter interface with FPGA
- On-board SRAM (16Mbit) and Flash memory (128MBit) with shared address and 8 bit data interfaces to the FPGA
- On-board DRR3 memory (4 Gbit) with 16 bit data interface to FGPA
- Dual QSPI serial memory interfaces to FPGA with provision to mount two devices each of SPI flash (nominally *Micro technologies N25Q064A,* 64Mbit flash) and QSPI-MRAM (nominally *Everspin MR10Q010*, 1 Mbit MRAM)
- Header with configurable pull-up for a user defined two-wire I2C peripheral interface
- Additional connections to Xilinx GTX high-speed serial transceiver interfaces with SMA connectors
- On-Board power circuits for 3.3V, 1.8V, 1.5V, 1.0V, 1.2V_GTX, 1.0V_GTX, VTTDDR and Vcore for FPGA, generated from a single 5V(min) 12V (nom) 15V (max) voltage input.
- 128 Mbit QSPI memory circuit for non-volatile memory storage of FPGA configuration.
- Miscellaneous support components for clock, reset, indicators and bootstrap signals

Additionally, a mezzanine connector is provided with 80 additional general purpose connections to the FPGA (3.3V LVTTL/LVCMOS) to allow additional user defined circuits to be designed and implemented.

For this board, an example mezzanine board has been developed implementing:

- *Octal Serial ADC (AD7888)*
- *Four Serial DACs (AD9706)*
- *Atmel I2C Serial EEPROM with programming header (AT17LV010 TBC)*

To enable convenient connection to the interfaces, most connector types and pin-outs are compatible with the standard connector types for these types of interfaces.

1.2 References

RD-1 GR-CPCI-XC7K_schematic.pdf, Schematic

RD-2 GR-CPCI-XC7K_assy_drawing.pdf, Assembly Drawing

RD-3 GR-CPCI-XC7K_bom.pdf, Bill of Materials

RD-4 GRMON2 User Manual, Cobham Gaisler, part of GRMON2 package

RD-5 GR-MEZZ Technical Note, Technical Note about Mezzanine connectors

1.3 Handling

ATTENTION : OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This unit contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the unit observe appropriate precautions and ESD safe practices.

When not in use, store the unit in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the unit is in an un-powered state.

When operating the board in a 'stand-alone' configuration, the power supply should be current limited to prevent damage to the board or power supply in the event of an over-current situation.

This board is intended for commercial use and evaluation in a standard laboratory environment, nominally, 20°C. All devices are standard commercial types, intended for use over the standard commercial operating temperature range (0 to 70ºC).

1.4 Abbreviations

ADC	Analog to Digital Converter
CPCI	Compact Peripheral Connect Interface
DAC	Digital to Analog Converter
DIL	Dual In-Line
DIP	Dual In-Line Plastic
DSU	Debug Support Unit
ESD	Electro-Static Discharge
FP	Front Panel
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input / Output
I/O	Input/Output
IP	Intellectual Property
LED	Light Emitting Diode
LVDS	Low Voltage Digital Signalling
MUX	Multiplexer
PCB	Printed Circuit Board
QSPI	Quad-data Serial Peripheral Interconnect
SMD	Surface Mount Device
SPDT	Single Pole Double Throw
SPI	Serial Peripheral Interconnect
SPW	Spacewire
TBC	To be Confirmed
UPLI	UTMI+ Low Pin Interface

2 ELECTRICAL DESIGN

2.1 Board Block Diagram

The *GR-CPCI-XC7K* Board provides the electrical functions and interfaces as represented in the block diagram, Figure 2-1.

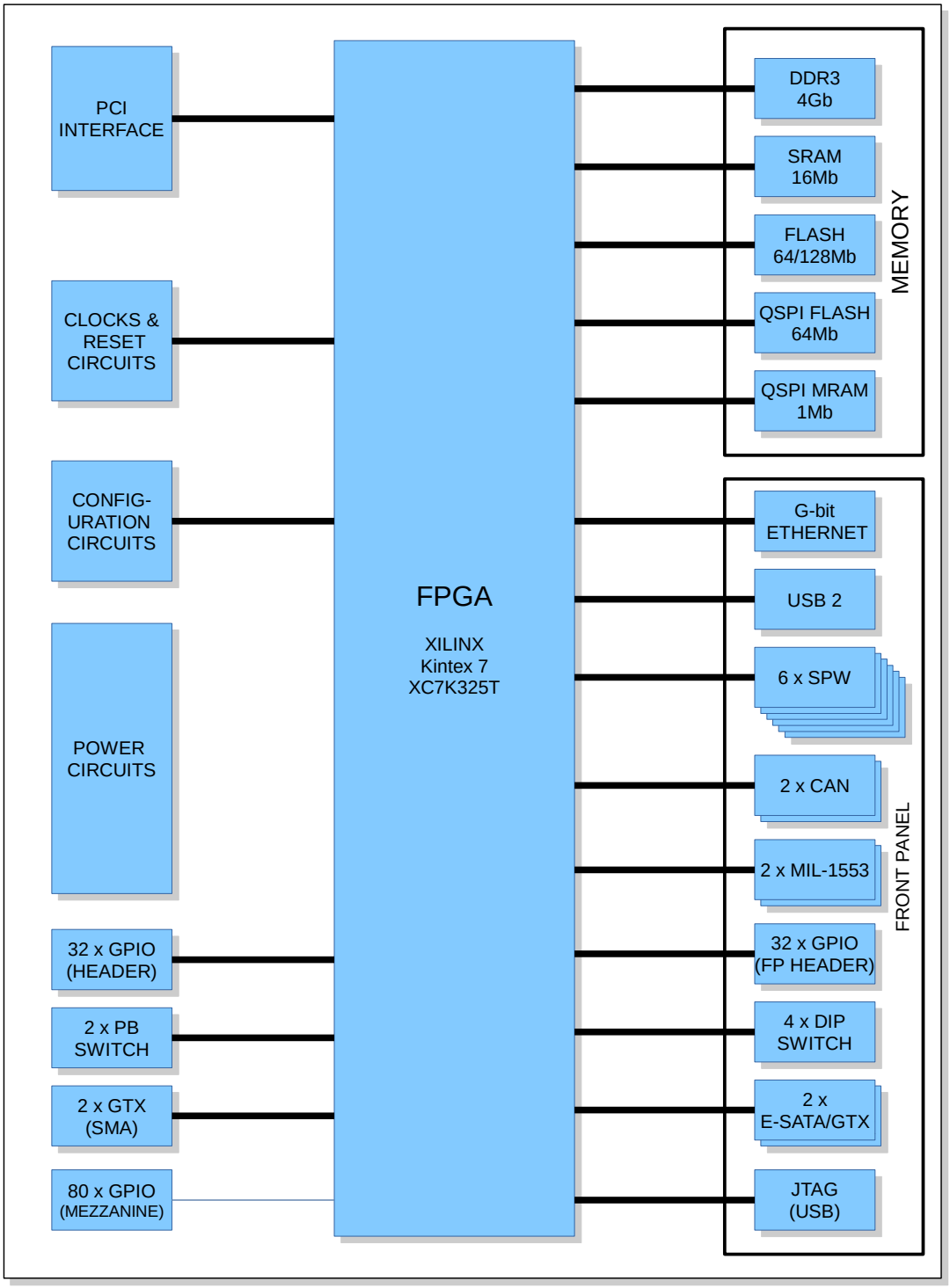

Figure 2-1: Block Diagram of GR-CPCI-XC7K board

2.2 Board Mechanical Configuration

The Main PCB is a 6U Compact PCI format board (233.5 x 160mm) and can be used 'stand-alone' on the bench-top simply using an external +5V power supply, or can be plugged in to a Compact PCI backplane.

Figure 1-1, shows the board as a stand alone PCB. However, for installation into a Compact PCI rack, this board is provided with a custom CPCI front panel with the appropriate connector cut-outs. The board equipped with the 6U, 2 slot wide CPCI front panel is shown in Figure 2-2.

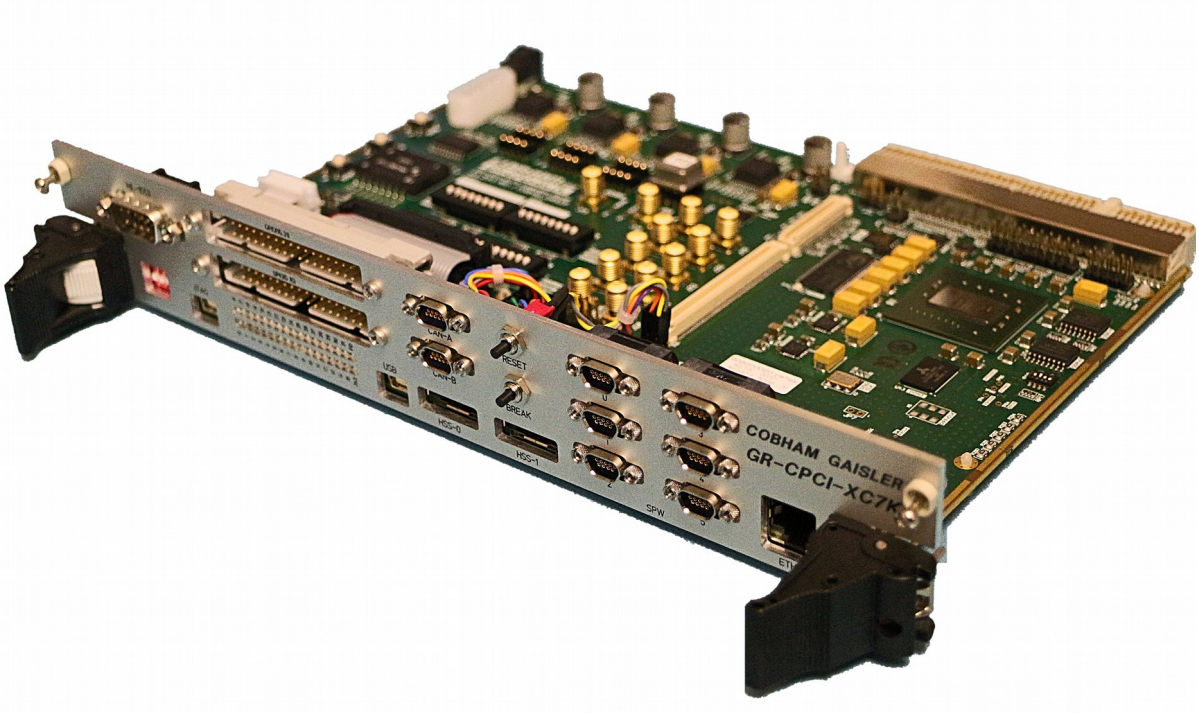

Figure 2-2: GR-CPCI-XC7K Board with CPCI Front Panel

Additionally, the board concept is compatible with its installation in a housing. This configuration requires the housing itself, and the replacement of the CPCI front panel with a custom front panel to suit the housing. The advantage of the housing is that it provides a robust and protected environment for the board, which would be suitable to allow its use in a desktop environment, for example during software development or evaluation. The disadvantage of the housing is that it restricts the access to some of the configuration features of the board (DIP switches or jumpers) and therefore may hinder the easy use of some of the features.

2.3 FPGA

The FPGA implemented on this board is a *Xilinx Kintex7 XC7K325T* in a 900 ball 1mm pitch package.

The footprint of this device is also compatible with the larger *Kintex7 XC7K410T* device which could be substituted if a larger FPGA device is desired.

The details of the interfaces, operation and programming of the *Xilinx* FPGA devices are described extensively in the *Xilinx* documentation and are not further referenced in detail in this document.

2.4 Memory

The organisation of the on-board memory and its connection to the FPGA is represented in Figure 2-3.

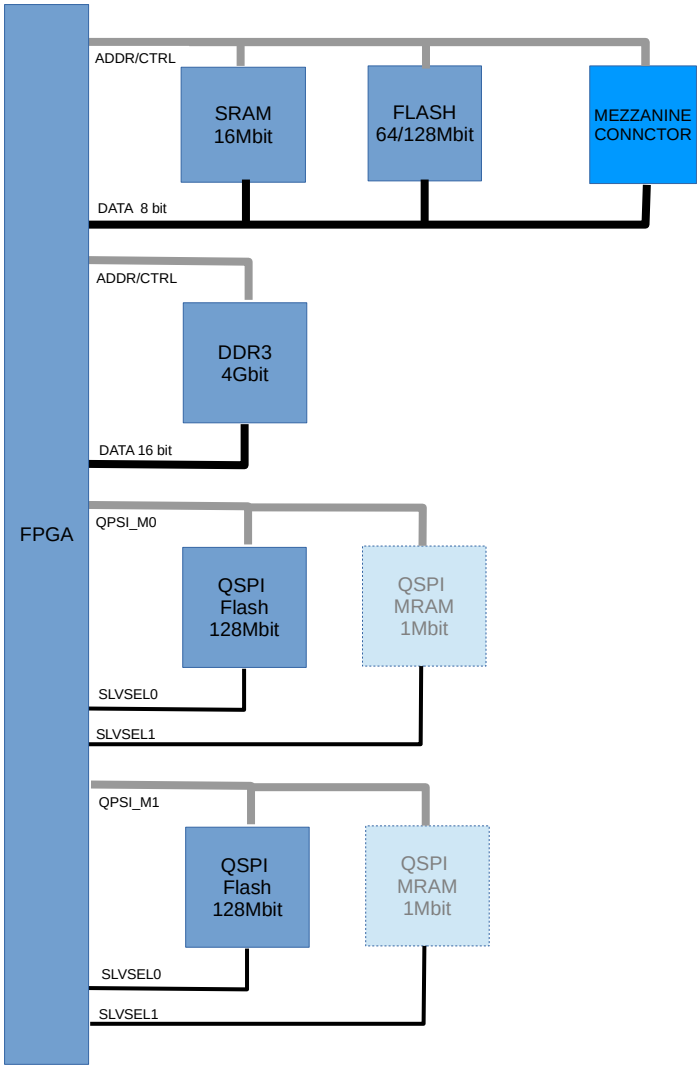

Figure 2-3: On-Board Memory of GR-CPCI-XC7K board

2.4.1 Flash

A 64Mbit or 128Mbit Flash EPROM is implemented with a single *Micron JS28C640J3* or *JS28C128J3* device with an 8 bit data interface to the FPGA.

The address and data interface signals are shared with the parallel SRAM memory.

2.4.2 SRAM

A 16Mbit SRAM is implemented with a single CY7C1069, 10ns SRAM device with an 8 bit data interface to the FPGA.

The address and data interface signals are shared with the parallel Flash memory.

2.4.3 DDR3

DDR3 memory (4 Gbit) is implemented with a single Alliance Semiconductor *AS4C256M16D3L* (or equivalent), with 16 bit data interface to FPGA. This device can operate either as DDR3 (1.5V) or DDR3L (1.35V) depending on the whether DC/DC converter U35 is set for 1.5V or 1.35V (Default is determined by the resistor soldered on the board to be 1.5V).

The interface between DDR3 device and FPGA utilises two High Performance I/O Banks (HP), and the pin definition has been derived using the Xilinx MIG generator tool.

2.4.4 Quad SPI

Dual QSPI serial memory interfaces to the FPGA are provided with provision to mount two devices each of SPI flash (nominally *Micron technologies N25Q064A,* 64Mbit flash) and optionally QSPI-MRAM (nominally *Everspin MR10Q010*, 1 Mbit MRAM)

2.5 PCI Interface

The *GR-CPCI-XC7K board* incorporates a 33/66MHz/32 bit interface with 4 channel PCI Arbiter and is capable of being configured to be installed in either the SYSTEM slot (HOST) or in PERIPHERAL slots (GUEST).

The *GR-CPCI-XC7K board* board can be configured to operate either as a peripheral slot card or system slot card as described in the following sections.

Note that the *GR-CPCI-XC7K board* has been designed to operate in a 3.3V signalling environment, and the Compact PCI connector is appropriately keyed (yellow key).

2.5.1 Host/System Slot Configuration

When installed in the System slot, the board provides the PCI arbitration and distributes the required PCI clocks to the backplane, and to the PCI interface in the FPGA.

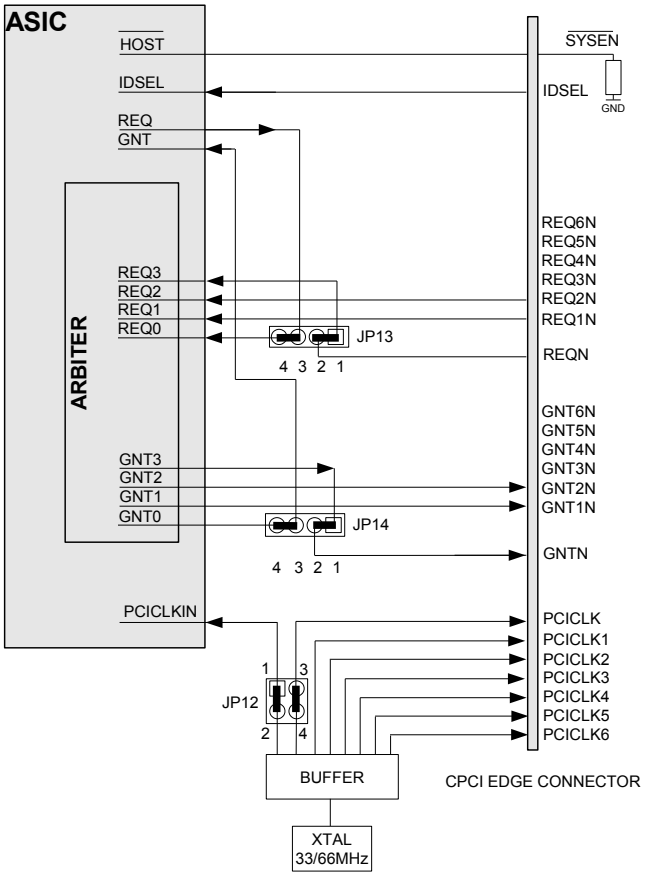

Figure 2-4: Block diagram for PCI System Slot connections

This requires the jumpers to be installed as follows:

JP12	1-2 and 3-4
JP13	1-2 and 3-4
JP14	1-2 and 3-4

Additionally, the PCI specification requires that the following system signals are pulled-up by

the card operating in the system slot:

PCI_FRAMEN	PCI_IRDYN	PCI_TRDYN	PCI_DEVSELN
PCI_STOPN	PCI_PERRN	PCI_SERRN	PCI_LOCKN
PCI_PAR	PCI_IDSEL		

This can be achieved by installing the JP11 jumpers 1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, 15-16, 17-18 and 19-20.

The jumper JP15 should be installed if it is required to force the PCI interface to operate with 33MHz bus speed.

2.5.2 Peripheral Slot Configuration

When functioning in a Peripheral slot, the board receives its input clock from the backplane, and connects its REQN/GNTN signals to the backplane REQN/GNTN signals.

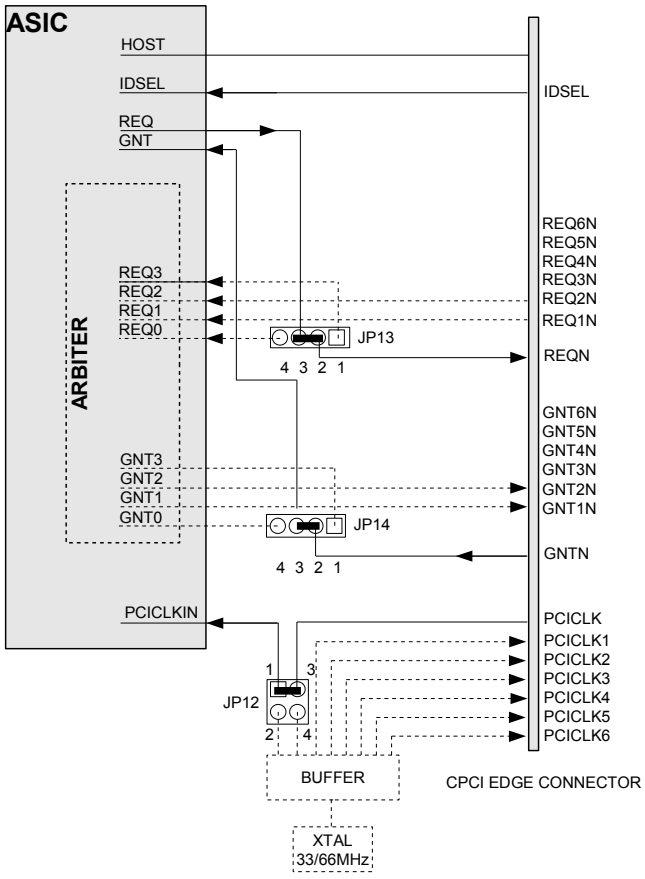

Figure 2-5: Block diagram of PCI Peripheral connections

This requires the jumpers to be installed as follows:

JP12	1-3
JP13	2-3
JP14	2-3

None of the jumpers in JP11 and JP15 should be installed.

2.5.3 33 / 66 MHz PCI Bus Speed

The *GR-CPCI-XC7K board* is capable of operating either with a 33 MHz or 66 MHz PCI bus

speed. If operating as a Host in the System slot, the *GR-CPCI-XC7K* Board is required to provide the PCI Clock to the other slots via the Backplane and an oscillator must be provided on the board (X6). To enable either 33 MHz or 66 MHz to be used, this oscillator is socketed and the user can exchange and install the correct oscillator, as appropriate.

A backplane pin M66EN pin is connected to the ASIC, and is intended in the PCI specification to signal to the PCI-Host whether the Backplane/System is capable of operating at 66MHz clock frequency. In principle this could be used to automatically select whether a 33MHz or 66MHz clock is used for the PCI interface. However, there is no mechanism on this board to automatically change this frequency, and the User is instead required to install the desired Oscillator in socket X6 in order to use either 33 or 66 MHz as the PCI frequency when in PCI-Host mode. Note also that 66MHz clocking of PCI is in principle only valid for systems with a maximum of 5 slots.

If, in a system capable of 66MHz bus speed, it is for some reason it is required to run the bus at 33MHz, this can be achieved by installing the Jumper *JP15*, which will force the M66EN of the backplane to DGND.

2.6 Ethernet Interface

The *GR-CPCI-XC7K board* device incorporates an Ethernet controller with support for GMII and MII interfaces, with a Micrel *KSZ9021GN* 10/100/1000Mbit/s Ethernet PHY transceiver. These is connected to a RJ45 connector at the front panel (J7)

For more information on the registers and functionality of the Ethernet MAC+PHY device please refer to the data sheet for the *KSZ9021GN* device.

The GMII Ethernet PHY has a local 25MHz crystal (Y1).

The Ethernet Interface has a hard-wire PHY Address of 1 (“001”) on this board.

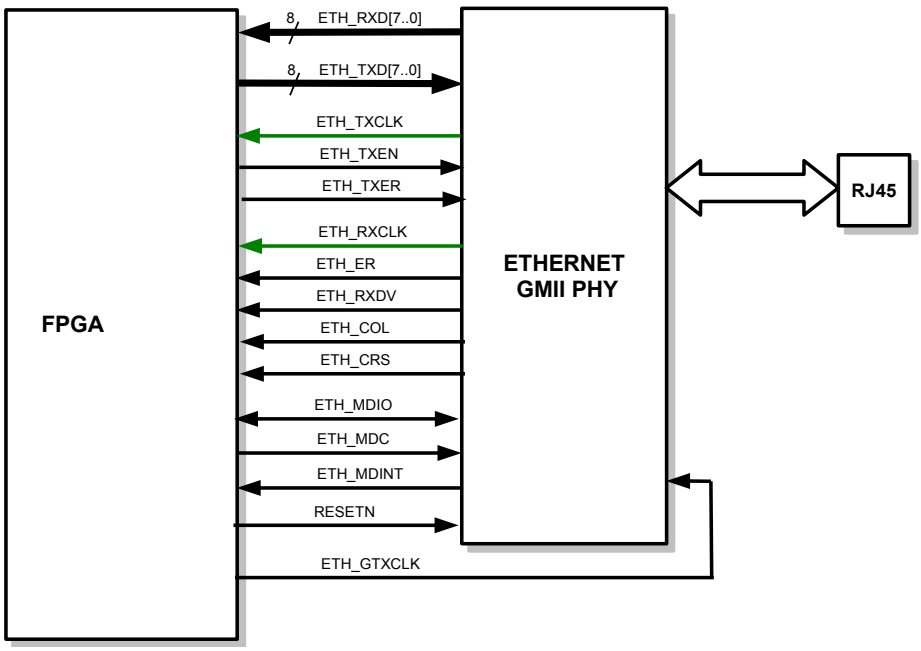

Figure 2-6: Block diagram of Ethernet GMII/MII Interface

2.7 Spacewire (LVDS) Interfaces

The *GR-CPCI-XC7K board* provides six Spacewire interfaces which are routed to the front panel of the board.

2.7.1 SPW interface circuit

Each Spacewire interface consists of 4 LVDS differential pairs (2 input pairs and 2 output pairs). As the Spacewire interface to the *GR-CPCI-XC7K board* is LVCMOS (3.3V logic), LVDS driver and receiver circuits are required on the PCB to interface between the ASIC and the external interface.

On-board LVDS transceivers (*TI, SN65LVDS050PW*) are provided for these six interfaces.

The PCB traces for the LVDS signals on the *GR-CPCI-XC7K board* board are laid out with 100-Ohm differential impedance design rules and matched trace lengths.

100 Ohm Termination resistors for the LVDS receiver signals are mounted on the board close to the receiver.

2.7.2 SPW Connectors

In order to be compatible with other SPW equipment, standard MDM9S connectors are mounted on the CPCI front panel for the Spacewire interfaces. The pin out of the MDM9S connectors for these Spacewire interfaces conform to the Spacewire standard. In order to make the transition from the PCB to the front panel, 40 pin high speed SAMTEC connectors together with a small flex-prints are used, as shown in Figure 2-7.

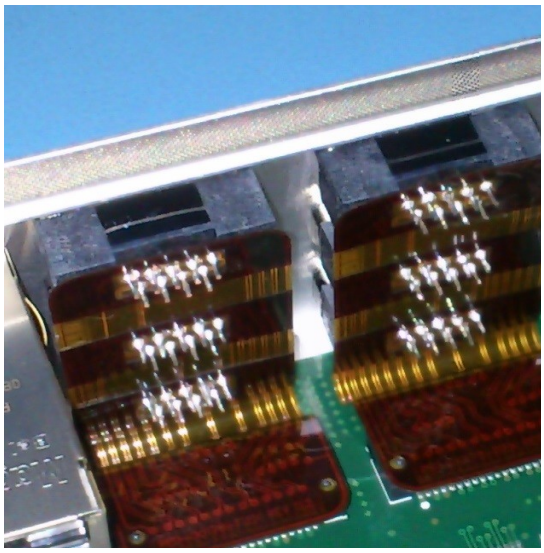

Figure 2-7: SPW flex connection

2.8 USB 2.0 ULPI Interface

A USB Device link is provided on the board (Connector J2) with an on-board USB PHY (*Micrel USB3340*) which is connected to I/O pins on the FPGA.

The interface between the USB-PHY and the FPGA is ULPI with a clock frequency of 60MHz. Please refer to the device data sheet of the *USB3340* device for further information

about the USB PHY device.

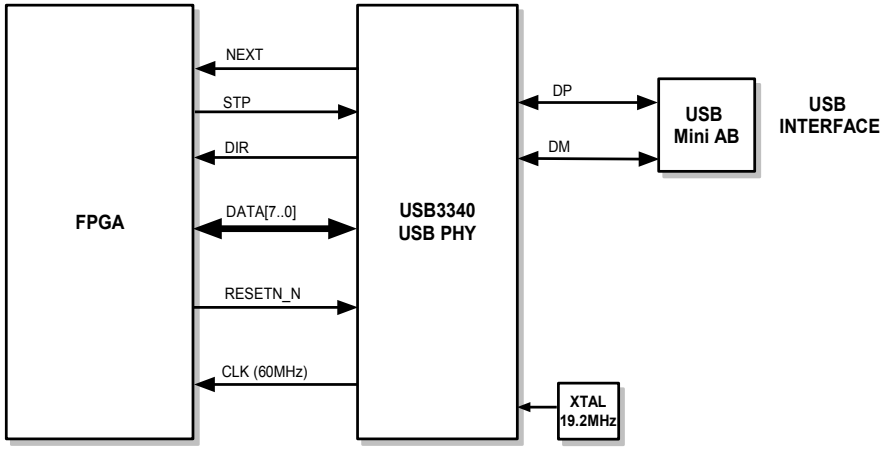

Figure 2-8: USB Host Controller PHYsical Interface

2.9 CAN Interfaces

The PCB provides the electrical interfaces for two CAN bus interfaces, as represented in the block diagram, Figure 2-9.

The CAN bus transceiver IC's on this board are *SN65HVD230* devices from Texas Instruments which operate from a single +3.3V power supply.

On the board, two 10 pin headers are provided for these CAN interfaces. This header can be connected to a User's choice of CAN connector using simple crimp and wire connection. However, for this development the connector type has been defined to be MDM9 Female which is provided on the front panel. The pin-out follows the standard pin out numbering (ref. Table 4-2 And Table 4-3) for CAN connections.

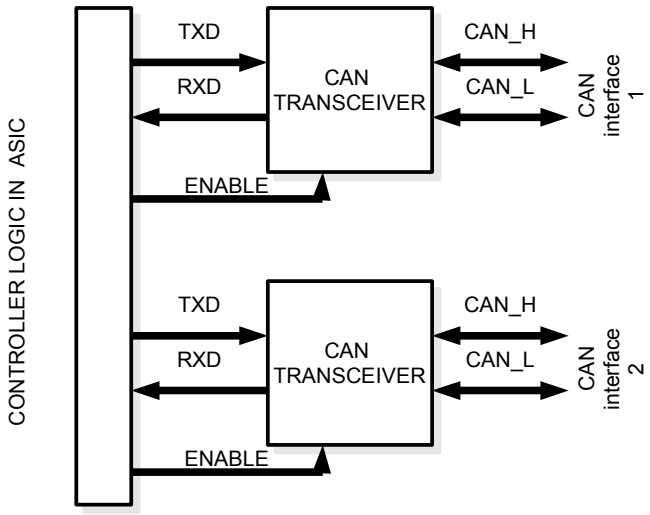

Figure 2-9: Block Diagram of the CAN interface

2.9.1 Configuration of Bus Termination

The CAN interfaces on the board can be configured for either end node or stub-node operation by means of the jumpers JP1 and JP2 for interface 1 and 2 respectively, as shown in Figure 2-10.

For normal end-node termination with a nominal 120 Ohm insert jumpers in position 1-3.

However, if a split termination is desired (if required for improved EMC performance), insert the jumpers in positions 1-2 and 3-4.

For stub nodes, if termination is not required, do not install any jumpers.

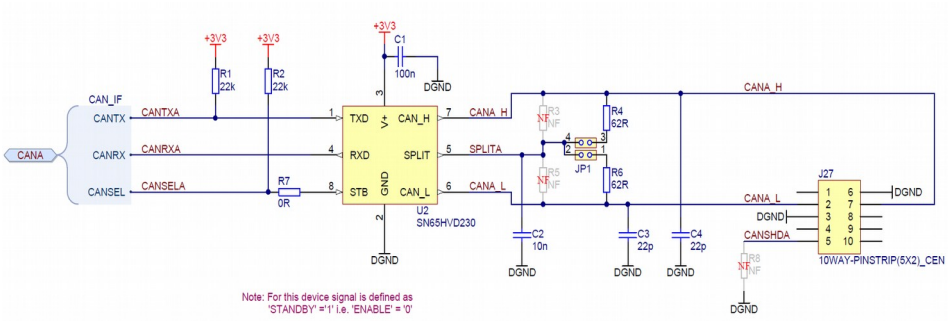

Figure 2-10: Transceiver and Termination Configuration (one of 2 interfaces shown)

2.9.2 Configuration of Enable/Standby Mode

The SN65HVD230 transceiver device used on the board has the facility to set the device into either *STANDBY* mode, by connecting an active high external signal to pin 8 of the device (refer to Figure 2-10). This means the FPGA should drive *CANSEL* inputs to low in order to enable the transceivers.

A further feature provided by the SN65HVD230 device is the capability to adjust the transceiver slew rate. This can be done by modifying the values of resistors connected to pin 8 of the transceivers.

The default value of 0 ohms is compatible with 1Mbps operation.

From the data sheet the following resistor values give the following slew rates:

10kOhm => 15V/us

100kOhm => 2V/us

2.10 High Speed Serial IO / E-SATA GTX Interfaces

Two High Speed Serial interfaces are prpvided with two E-SATA front panel connectors which are connected to two Xilinx GTX high-speed serial transceiver interfaces of the FPGA.

Additionally, 8 SMA connectors (J19 to J26) provide connections to two additional RX/TX GTX transceiver interfaces of the FPGA.

2.11 Dual MIL-1553 Interface

The board implements a Dual MIL-STD-1553 interface with a 3.3V Transceiver and Transformer circuits as shown in Figure 2-11.

The default configuration of the board supports Long-Stub Coupling configuration. However,

short-stub and direct-coupling can also be supported depending on the configuration of resistors which is soldered to the board (see Figure 2-11). Additionally, a 80 Ohm parallel termination can be installed if the 2 pin jumpers are installed.

Since there are various 'standard' connectors defined for the connection to MIL-STD-1553 bus, and because of limited PCB area, it has been decided to implement 10 pin header on the board. This can be easily connected to a D-sub 9-Male connector on the front panel using a short ribbon one-to-one cable connection (see Figure 2-12). A D-sub 9-Male connector on the front panel is selected as this can be most easily adapted to suit the user's desired connector configuration.

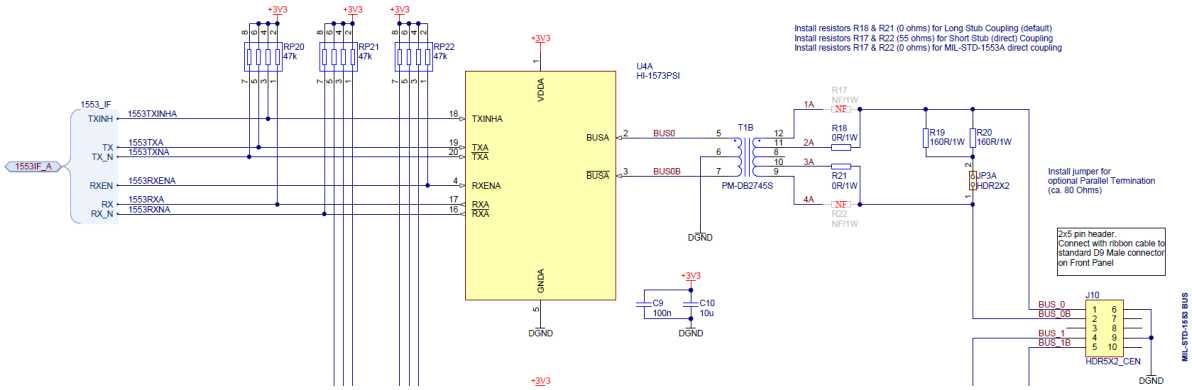

Figure 2-11: MIL-STD-1553 Transceiver and Transformer circuit
(one of two interfaces shown)

Note: Concerning routing on the PCB: Underneath the transformer and associated traces of the MIL-1553 circuit, the PCB planes in the internal layers have been 'removed', and no other traces are routed through this area of the PCB. This is done in order to eliminate any magnetic coupling from the transformer circuit in to the Ground plane.

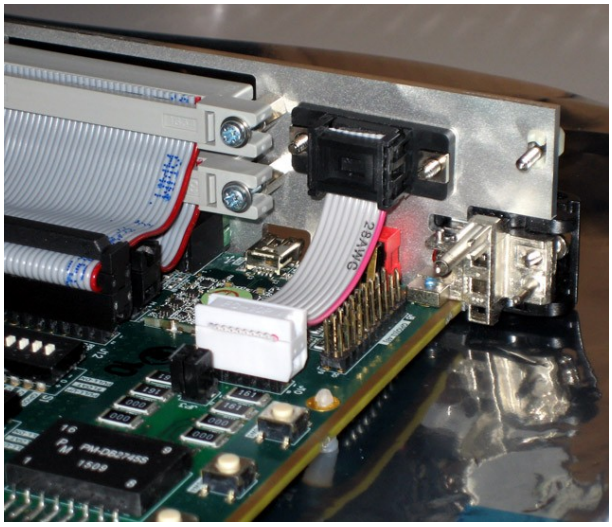

Figure 2-12: Ribbon cable connection to front Panel D-SUB connector

2.12 GPIO

The *GR-CPCI-XC7K ASIC* provides 32 general Purpose Input Output signals (3.3V LVCMOS voltage levels).

On the *GR-CPCI-XC7K*, each GPIO pin is connected to the following circuits as represented in Figure 2-13.

- to a double-throw switch which allows the pin to 'float', 'pull-up to 3V3' or 'pull-down to DGND'. The pull-up/pull-down value is a weak 47k.
- connected to a header on the board to allow easy access for measurement This header, in turn can be connected with a short ribbon cable to a corresponding header on the front panel (Figure 2-14). A series protection resistor of 470 Ohm is included on each signal to provide a simple level of protection in the case of a short circuit at the front panel
- connected to a front panel LED (via an inverting driver) to indicate the state of the pin at the ASIC

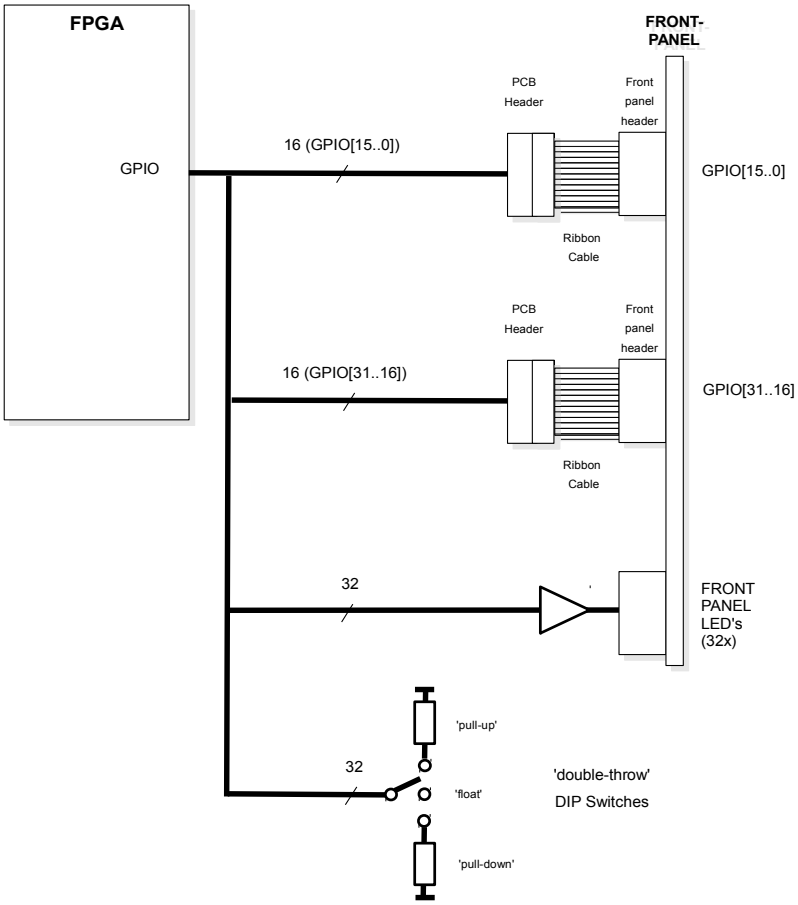

Figure 2-13: GPIO interface configuration

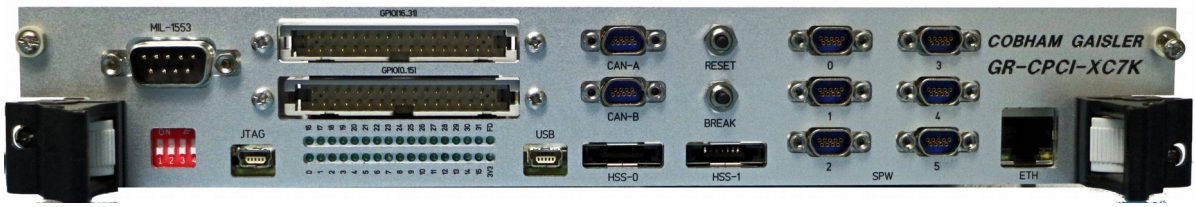

Figure 2-14: Front Panel GPIO connections

An additional 32 General Purpose I/O signals on two 20 pin headers (*J8* and *J9*), compatible with ribbon cable connections with *GR-Accessory* boards (e.g. RS232 UART) are provided.

A header (*J32)* user-defined two-wire I2C peripheral interface (*USER_SCL* and *USER_SDA*) is provided. These pins are pulled up to 3.3V with 10k resistors.

2.13 Auxiliary Mezzanine

The board implements a two mezzanine connector, to allow user-designed logic to be implemented on a mezzanine board.

A 120 pin mezzanine connector (*Tyco AMP 5177-984-2*) provides connections to 80 dedicated FPGA I/O pins with 3.3V LVTTL/LVCMOS voltage levels.

The pin out of this connector is represented in Figure 2-15.

The connections to the FPGA nd the routing of the PCB allows these mezzanine signals to be used as either 80 single ended I/O signals, or as 40 differential pairs (or combination thereof).

A second 60 pin mezzanine connector (*Tyco AMP 5177-984-2*) implements an memory interface to allow external 8bit wide memory devices to be connected to the Flash/SRAM Memory bus.

The pin out of this connector is represented in Figure 2-16.

Please note that this pin ordering as used on this board (Figure 2-15 & Figure 2-16) does not match exactly the pin ordering which you will find on the Tyco part datasheets for the Mezzanine board mating connectors. The reason for this is explained in more detail in the Technical Note, RD-5.

Therefore please take care when designing your own mezzanine boards to take account of this pin ordering.

If there is any confusion, or you have any doubts, please do not hesitate to contact info@pender.ch. Additional dimensional data or Gerber layout information can be provided, if required to aid in the layout of the User's mezzanine board.

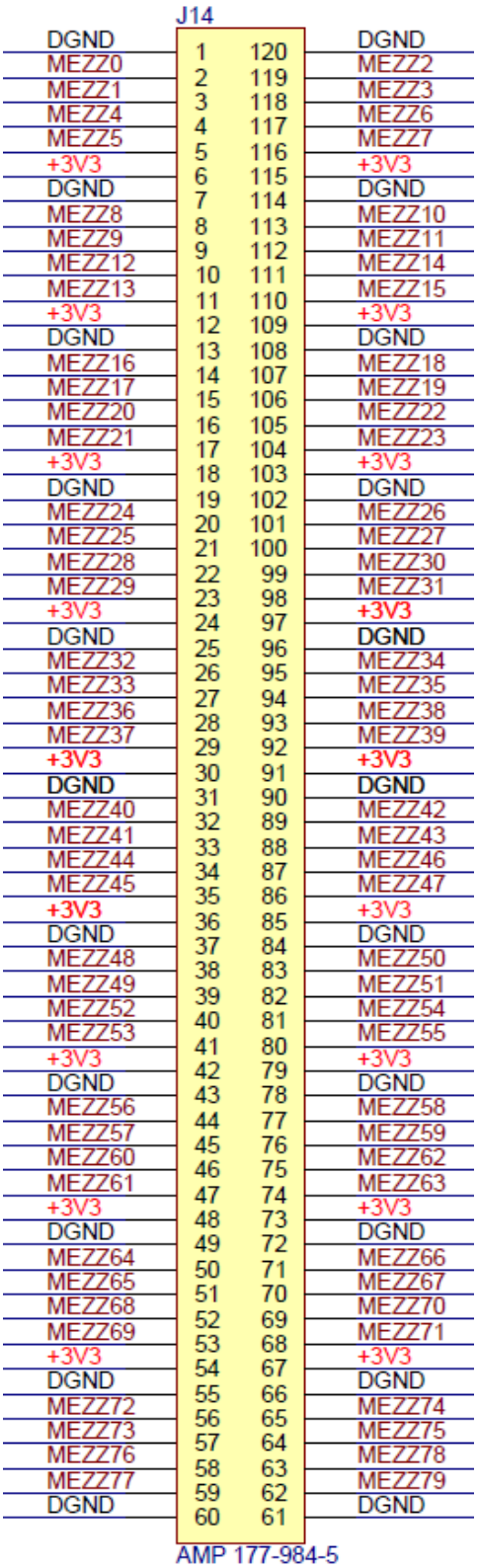

Figure 2-15: Mezzanine Connector for User Defined Functions

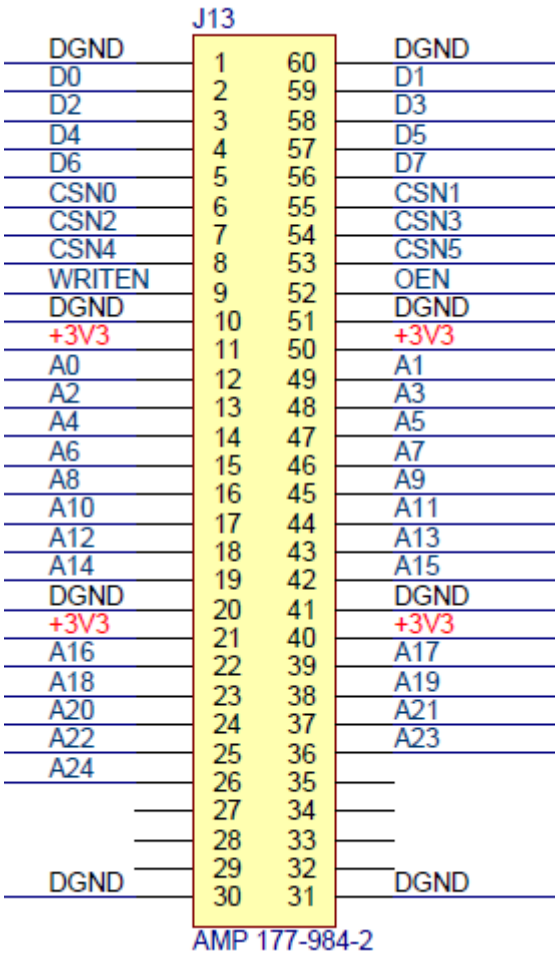

Figure 2-16: Mezzanine Connector for 8 bit external memory interface

2.14 Other Auxiliary Interfaces and Circuits

2.14.1 Oscillators and Clock Inputs

The oscillator and clock scheme for the *GR-CPCI-XC7K* Board is shown in Figure 2-17.

The main oscillator providing the *SYS_CLK* for the *GR-CPCI-XC7K* ASIC is a 50 MHz Crystal oscillator. To enable different oscillator frequencies to be used, a DIL socket is provided which accepts 4 pin DIL8 style 3.3V oscillator components.

Additionally, oscillators are provided as follows:

- *SPW_CLK:* DIL Socket for 100 MHz (TBC) oscillator to provide a separate clock for the Spacewire interfaces
- *PCI_CLK:* DIL Socket for 33 or 66 MHz (TBC) oscillator to provide a separate clock for the PCI interface
- CLK_1553: 24 MHz oscillator intended for clocking the 1553 interface
- An option is foreseen to mount a soldered SMD oscillator on the board. This oscillator would be a 1.8V type with LVDS output. This could be useful if a specific oscillator is needed whose frequency exceed the 100MHz available in the DIL socket types.

For the clocking of the GTX features fo the FPGA, three clocking options are foreseen:

1. SMA connectors to allow an external differential clock to be applied from external test equipment. This should typically be a LVDS clock, and is AC coupled to the GTX clock input.
2. A dedicated 156.25 MHz oscillator is soldered on to the board. This is a differential LVDS type with 1.8V power supply, and is AC coupled to the GTX clock input.
3. Two output pins of the FPGA are connected to a differential clock input of the GTX circuits with an AC coupling. The intention is that logic inside the FPGA can be used to generate an LVDS clock signal for this purpose with a user-defined frequency

The following additional clocks are required by peripherals on the board and should be generated using the MMCX clock management features inside the FPGA:

- ETH_GTX_CLK (LVCMOS 3.3V) 125 MHz
- DDR3 clock (Differential SSTL 1.5V), frequency TBD

For more details of the internal clock management features of the FPGA please refer to the Xilinx documentation.

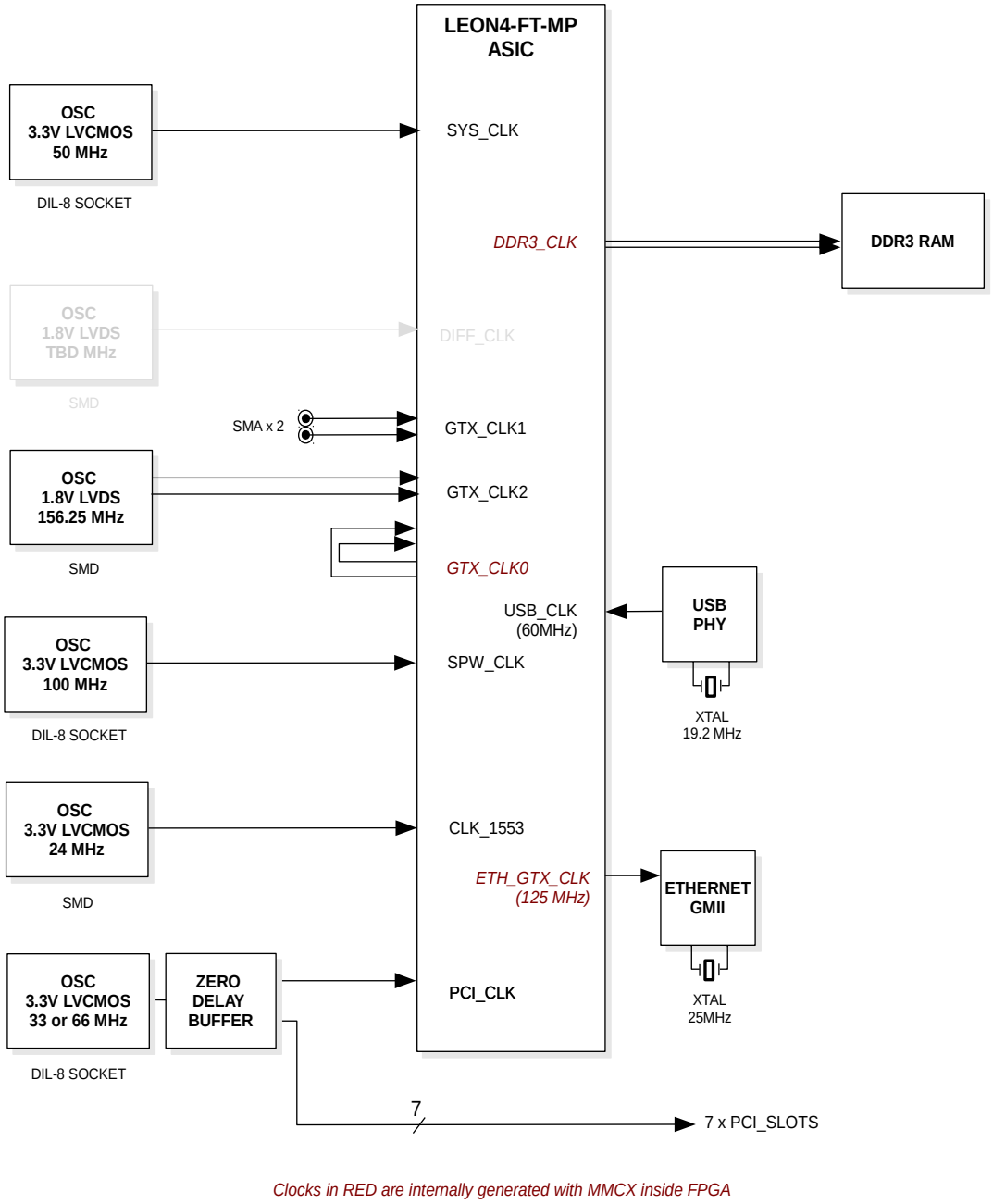

Figure 2-17: Board level Clock Distribution Scheme

2.14.2 Power Supply and Voltage Regulation

A single power supply with a +12V (nominal) is required to power the board. All other necessary voltages on the board are derived from this input using discrete Power circuits on the board (DC/DC or Linear Regulators as appropriate).

On board regulators generate the following voltages:

- +1.0V for the FPGA VCC_CORE voltage
- +1.8V for the FGPA VCC_AUX voltages
- +3.3V for the FPGA I/O voltage, interfaces and other peripherals
- +1.5V for the FPGA I/O and DDR3 circuitry
- +1.2V linear regulated supply for the GTX transceiver interfaces
- +1.0V linear regulated supply for the GTX transceiver interfaces
- +0.75V linear regulated supply for the DDR3 termination circuitry

Appropriate decoupling capacitance is provided for all the supply voltages.

The power supply concept is shown in Figure 2-18.

The Power Supply structure is comfortably dimensioned using 7A power modules (*LMZ31707*) as the basis, in order to provide for uncertainty and flexibility. The advantage of the selected DCDC power modules is their ease of implementation and the wide allowable input voltage range (+4.5V to +17V).

The values marked on this figure for the power supply currents are the 'capability' of the circuits being used, and do not necessarily indicate the actual expected current drawn from the supplies.

The actual currents expected, and hence the required input current for the board depend on the logic complexity and clock frequencies of the logic programmed into the FPGA are and are hence currently *TBD*.

Input Voltage

The LMZ31707 power converters have an allowable voltage input range from +4.5V to +17V.

The nominal input voltage for the board is intended to be +12V, but could be powered from a supply in the range +5V to +15V.

This input voltage can be connected to the 2.1mm Jack connector, *J11* on the board. An additional power input connector *J10* is provided on the board, as an alternative to the connector *J11.* This could be useful as a more convenient connection in the situation that the board would be built in to a 'stand-alone' equipment housing.

In the situation that the board is installed, in a CPCI rack, the main power input to the board is taken from the +5V PCI rail from the PCI Backplane.

Note: You must not apply power to the connector J10/J11 when the board is plugged into a CPCI rack.

Power Sequencing

Based on the Xilinx datasheet and application notes the required power up sequence recommended for the FPGA is:

1. VCCINT (1.0V)
2. VCCAUX (1.8V)
3. VCCIO (1.8V, 1.5V, 3.3V)

The LMZ31707 power regulators provide a '*Power Good*' output signal which can be used to signal and control the '*Inhibit*' input of a subsequent power converter. These signals are therefore are daisy chained to provide the necessary sequencing.

CPCI +/-12V Supply

The +12V and -12V (500mA max) power supply which the compact PCI can provide via the Backplane is not used on this board.

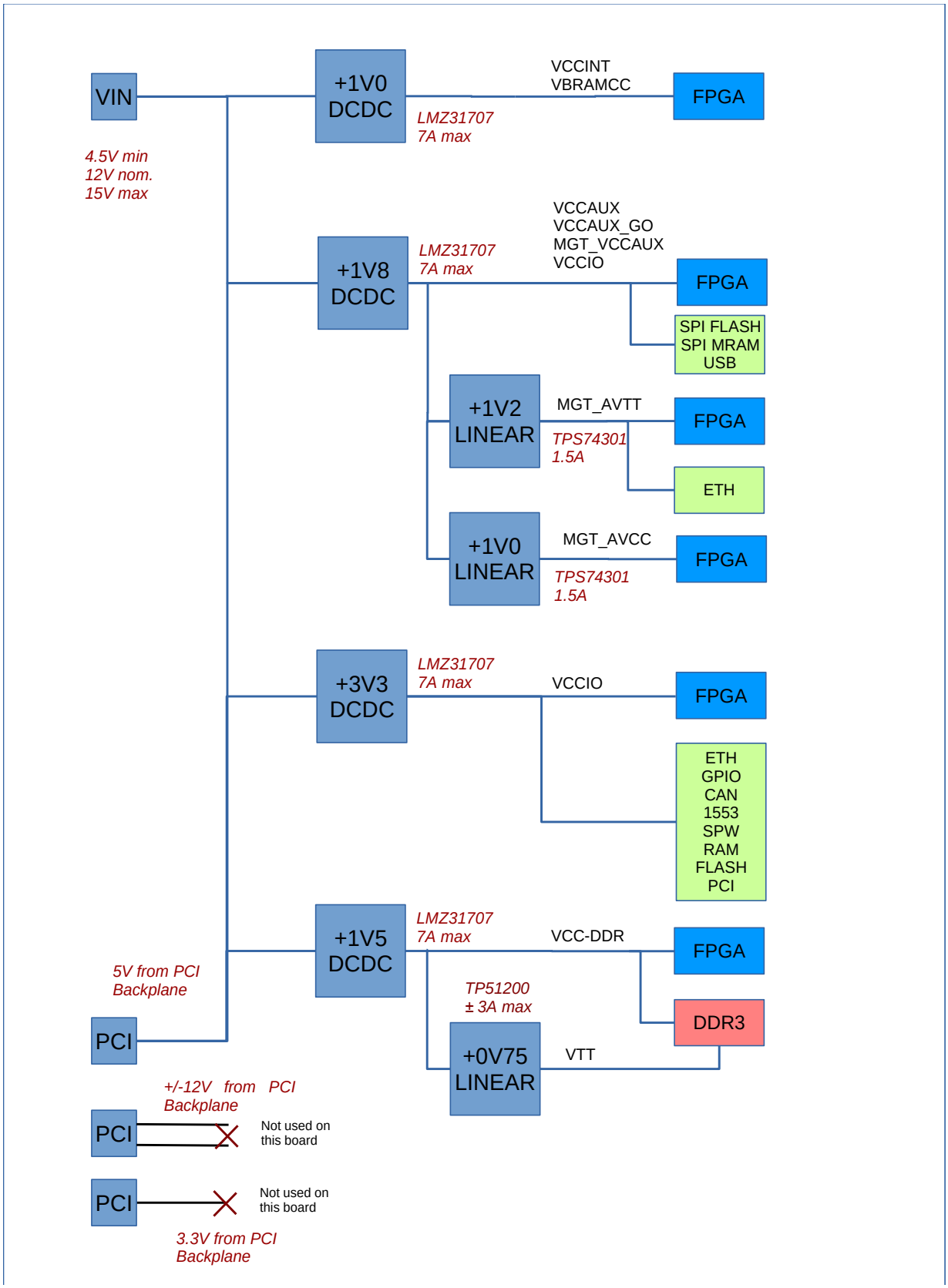

Figure 2-18: Power Regulation Scheme

2.14.3 Reset Circuit and Button

A standard Processor Power Supervisory circuit (TPS3705 or equivalent) is provided on the Board to provide monitoring of the 3.3V power supply rail and to generate a clean reset signal at power up of the Unit.

To provide a manual reset of the board, a miniature push button switch is provided on the Main PCB for the control. Additionally, connections are provided to an off-board push-button *RESET* switch on the front panel, if this is required.

2.14.4 Switches and Push-Buttons

- DIP switch with 4 switches, accessible from the front panel connected to I/O pins on the FPGA for 'user defined' purposes.

- Two miniature push buttons on the PCB connected to I/O pins on the FPGA for 'user defined' purposes. Additionally, a two pin header for each of these switches would allow a front panel push button switch to be connected (this is foreseen to allow one of the switch inputs to be used for a '*DSU Break'* function on the front panel.

2.14.5 LED and Indicators

In addition to the 32 LED indicating the GPIO status (see section 2.12) two additional front panel LED's are provided on the front panel to indicate the '*POWER'* and '*FPGA DONE*' status.

2.15 FPGA Programming and Configuration

2.15.1 JTAG programming

This board incorporates an on-board JTAG programming circuit with a *Digilent SMT2-NC module.*

A simple Mini-USB cable connection from Laptop to the J1 connector on the board allows the Xilinx Impact JTAG programming tools to be used to program and interrogate the FPGA via the JTAG interface. No additional external JTAG programming cable is required.

Upon connecting the board to lap-top, the *Digilent SMT2-NC module* should be automatically detected and the Xilinx tools should be able to connect to the board, assuming that a recent version of ISE/Vivado has been installed (v14.7 or higher).

Start the Xilinx iMPACT utility and select *Configure Devices / Boundary Scan Mode / Automatically connect to cable and identify Boundary-Scan chain.* The JTAG chain should be detected as shown in the Figure 2-20.

The following screenshot shows iMPACT version 14.6 running on Windows and the XC7K325T FPGA being correctly detected. The exact menu structure, layout etc., may depend on the version of ISE/Impact that you are using and the operating system.

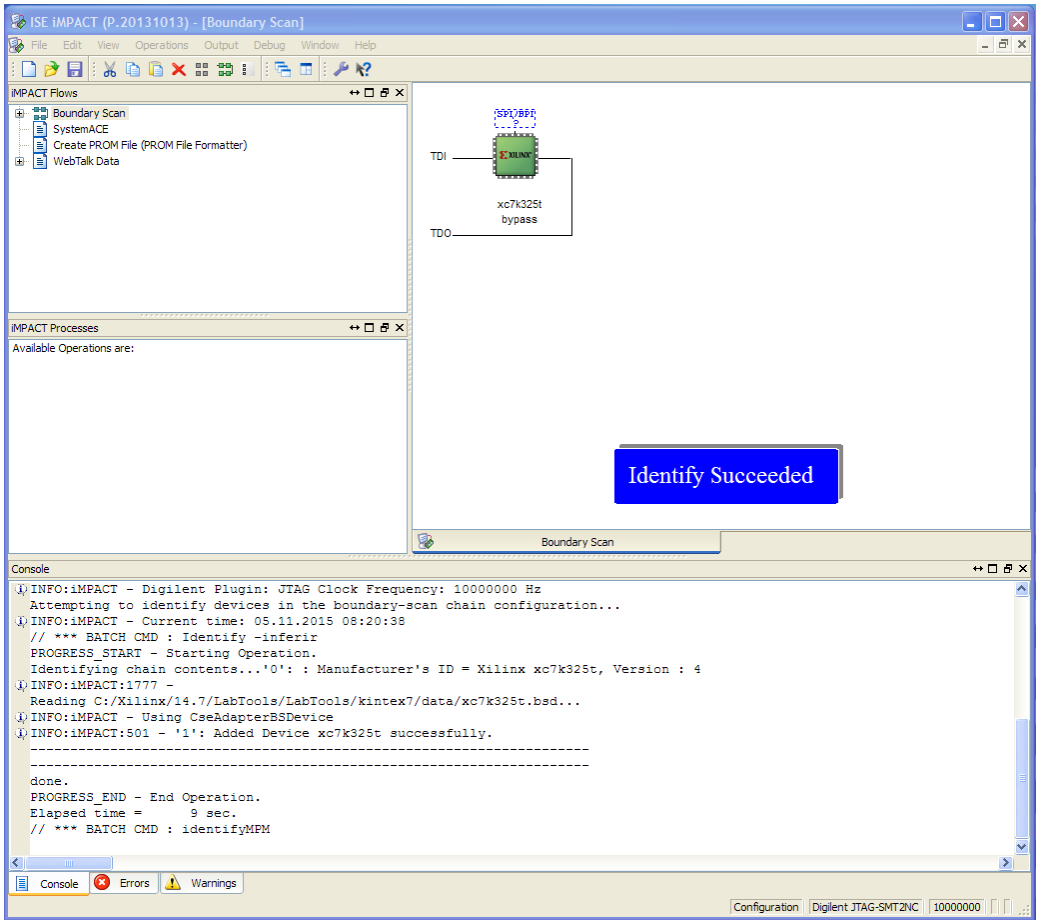

Figure 2-20: Initial JTAG chain configuration

2.15.2 Programming the SPI-Serial Prom via JTAG in Indirect mode

The GR-CPCI-XC7K board also includes an on-board 128Mbit SPI prom for non-volatile memory storage of FPGA configuration.

However, this SPI Serial Configuration PROM is not directly visible in the JTAG programming chain as it does not have a JTAG interface

However, this Prom can be programmed using the Xilinx Impact software, by using the *'Indirect SPI/BPI Programming'* mode. This is indicated by the dashed box marked *'SPI/BPI'* as shown in the Figure 2-20.

In this mode, the iMPACT software temporarily loads a special configuration on to the FPGA which is used to control the correct programming sequence of the SPI or BPI prom which is attached to the FPGA.

The S25FL128 prom is a serial prom which can be operated in x1, x2 or x4 bit data modes. To program the SPI prom, click on the box 'SPI/BPI'. A further dialog box will appear (Figure 2-21)

The options in the box should be set to:

SPI Prom => S25FL128S
Data Width => 4 bits (for fastest configuration speed use the x4 option)

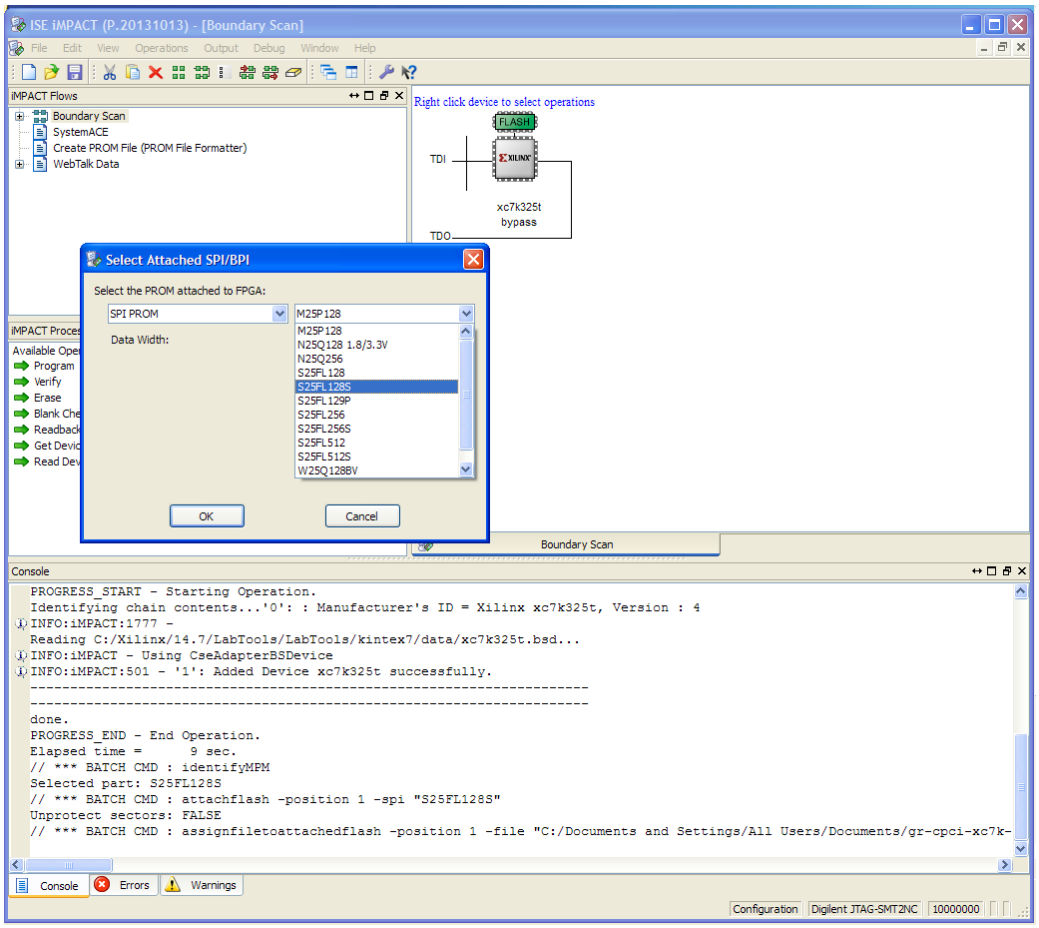

Figure 2-21: Indirect JTAG programming of Configuration Serial PROM

2.15.3 Automatic loading of FPGA Configuration at power-up

If a valid FPGA configuration has been programmed in the Configuration PROM, when the board is switched on the 'FPGA DONE' led (D17b on front panel) will extinguish briefly to indicate the start of the loading processes, and shortly afterwards, should illuminate indicating that the configuration is complete.

Note that the configuration speed depends on a number of configuration parameters – and can range from 2s to ca. 30s).

Note also that it is necessary to correctly set the FPGA boot mode using the miniature DIP switch S10. To load the configuration fro the SPI Configuration PROM, it is necessary to set the device to 'M*aster SPI Mode*'. = “001” on the Mode pins M[2..0] of the FPGA.

This requires DIP Switch S10 to be set to:

S10-3: closed => '0'

S10-2: closed => '0'

S10-1: open => '1'

3 SETTING UP AND USING THE BOARD

The default status of the Jumpers on the boards is as shown in Table 3-1. (Other configurations may be defined by the user).

For additional information, refer to RD 1.

Jumper	Jumper Setting	Comment
JP1	1-3 fitted	CAN termination 120 Ohm
JP2	1-3 fitted	CAN termination 120 Ohm
JP3	1-2 open 3-4 open	
JP4	Not fitted	
JP5	Connected to front panel button	User Button e.g. DSU Break
JP6	Connected to front panel button	Reset Push Button
JP7	Not fitted	
JP8	1-2 open	WP not enabled
JP9	JP9 1-2 fitted	PCI bus 33MHz
JP10	1-2 fitted	board generates RESETN
JP11	all fitted (1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, 15-16 17-18 19-20)	PCI Host
JP12	1-2 & 3-4 fitted	PCI Host
JP13	1-2 & 3-4 fitted	PCI Host
JP14	1-2 & 3-4 fitted	PCI Host
S1 1-8	Middle (float)	GPIO undefined
S2 1-8	Middle (float)	GPIO undefined
S3 1-8	Middle (float)	GPIO undefined
S4 1-8	Middle (float)	GPIO undefined
S9	Undefined	User Switches
S10	4: closed 3: closed 2: closed 1: open	PUDC_B ='0' => weak preconfig. pull-up resistors enabled For Master SPI Mode: Mode="001", FPGA generates CCLK, device is configured from SPI prom on power up.

Table 3-1: Default Status of Jumpers/Switches

To operate the unit stand alone on the bench top, connect the VIN power supply to the Power Socket J11 at the back of the unit. (centre-pin is +ve). The allowable voltage range is 5V to 15V with 12V being suggested as nominal (refer to section 2.14.2).

ATTENTION! To prevent damage to board, please ensure that the correct power supply voltage and polarity is used with the board.

Do not exceed +15V at the power supply input, as this may damage the board.

The *POWER LED* on the front panel should be illuminated indicating that the +3.3V power is active.

If an valid FPGA configuration is present in the Configuration PROM, the 'FPGA DONE' LED will illuminate shortly after power up (time depends on a number of configuration parameters – ranges from 2s to ca. 30s).

Otherwise, configuration of the FPGA can be performed using the JTAG interface and Xilinx Impact software.

4 INTERFACES AND CONFIGURATION

4.1 List of Connectors

Name	Function	Type	Description
J1	JTAG	USB-MINI-AB	JTAG programming interface
J2	USB	USB-MINI-AB	Mini USB connector for USB 2.0 interface
J3	HSS-0	E-SATA	E-SATA connector for GTX high speed serial interface
J4	HSS-1	E-SATA	E-SATA connector for GTX high speed serial interface
J5	SPW 0/1/2	Samtec QSE-20	Connects with flex-print to front-panel Spacewire conn (3x)
J6	SPW 3/4/5	Samtec QSE-20	Connects with flex-print to front-panel Spacewire conn (3x)
J7	GB-ETH	RJ45-100BASE-T	10/100/1G Mb Ethernet interface
J8	GPIO[47..32]	2x10 pin 0.1” Header	Expansion header for GPIO e.g. GR-ACC-6UART board
J9	GPIO[63..48]	2x10 pin 0.1” Header	Expansion header for GPIO e.g. GR-ACC-6UART board
J10	MIL-1553	2x5 pin 0.1” Header	Header connects to front panel D-SUB9 with ribbon cable.
J11	GPIO[15..0]	2x17 pin 0.1” Header	Expansion header for front panel GPIO
J12	GPIO[31..16]	2x17 pin 0.1” Header	Expansion header for front panel GPIO
J13	MEZZ-MEM	AMP 5177-984-2	60 pin mezzanine connector with 8 bit memory interface
J14	MEZZ-IO	AMP 5177-984-5	120 pin mezzanine connector for user mezzanine
J15	SPW-CLK	SMA-jack	SMA connector – for external SPW-CLK or monitor
J16	CLK	SMA-jack	SMA connector - for external CLK or monitor
J17	GTXCLK1_P	SMA-jack	SMA connector - GTX CLK1_P input
J18	GTXCLK1_N	SMA-jack	SMA connector - GTX CLK1_N input
J19	RX-DATA1_P	SMA-jack	SMA connector – GTX RX-DATA1_P output
J20	RX-DATA1_N	SMA-jack	SMA connector – GTX RX-DATA1_N output
J21	TX-DATA1_P	SMA-jack	SMA connector – GTX TX-DATA1_P output
J22	TX-DATA1_N	SMA-jack	SMA connector – GTX TX-DATA1_N output
J23	TX-DATA0_P	SMA-jack	SMA connector – GTX TX-DATA0_P output
J24	TX-DATA0_N	SMA-jack	SMA connector – GTX TX-DATA0_N output
J25	RX-DATA0_P	SMA-jack	SMA connector – GTX RX-DATA0_P output
J26	RX-DATA0_N	SMA-jack	SMA connector – GTX RX-DATA0_N output
J27	CAN	2x10 pin 0.1” Header	Expansion header for GR-CAN board
J28	SPI	2x6 pin 0.1” Header	Header for user SPI interface
J29	Power	2.1mm center +ve	Power (nominal +12V)
J30	Power	Mate-N-Lok 4pin	Power – 4 pin IDE style connector as alternative
J31	VIN-FAN	MOLEX_6410-2pin	2 pin header with Vin and GND connecitons (e.g. for FAN)
J32	USER-I2C	2x2 pin 0.1” Header	4 pin header for USER I2C connections (SCL/SDA)
CPCI-J1	CPCI	CPCI Type A	CPCI connector
CPCI-J2	CPCI	CPCI Type B	CPCI connector

Table 4-1: List of Connectors

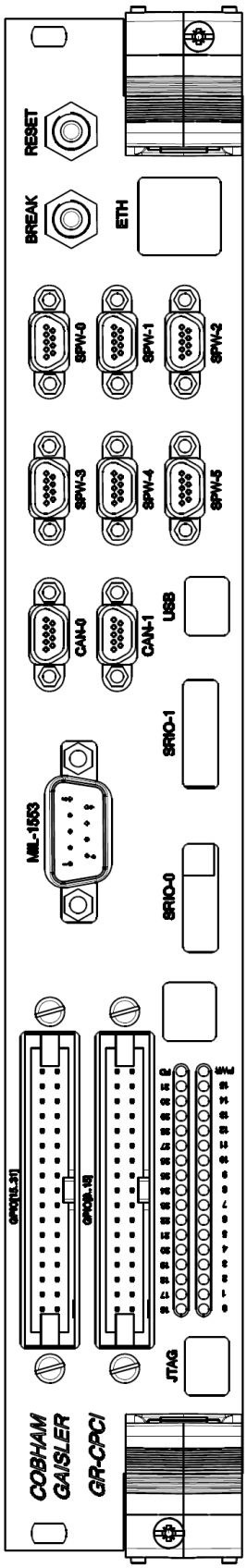

Figure 4-1: Front Panel View

4.2 List of Oscillators, Switches and LED's

Name	Function	Description
X1	1553-CLK	3.3V oscillator in 8 pin DIL format. Nominally 24MHz
X2	SPW-CLK	3.3V oscillator in 8 pin DIL format. Nominally 100MHz
X3	LVDS-CLK	LVDS differential clock, SMD soldered, 156.25MHz
X4	SYS-CLK	3.3V oscillator in 8 pin DIL format. Nominally 50MHz
X5	DIFF_CLK	Optional LVDS differential clock, SMD soldered, 'not-fitted'
X6	PCI-CLK	3.3V oscillator in 8 pin DIL format. Nominally 33MHz
Y1	ETH-XTAL	Ethernet PHY clock, 25MHz, SMD soldered
Y2	USB-XTAL	USB PHY clock, 12MHz, SMD soldered

Table 4-2: List and definition of Oscillators and Crystals

Name	Function	Description
D1-D16	GPIO	Front panel dual LED's indicating the status of the 32 bit GPIO signals.
D17a	DONE	Indicated configuration status of FPGA 'DONE' pin
D17b	POWER	3.3V power
D18	PROM-BUSY	Illuminated when Flash PROM is being written or erased.

Table 4-3: List and definition of PCB mounted LED's

Name	Function	Description
S1	GPIO[7..0]	8 pole double throw DIP switch; can be set to 'pull-up', 'pull-down' or 'float'
S2	GPIO[15..8]	8 pole double throw DIP switch; can be set to 'pull-up', 'pull-down' or 'float'
S3	GPIO[23..16]	8 pole double throw DIP switch; can be set to 'pull-up', 'pull-down' or 'float'
S4	GPIO[31..24]	8 pole double throw DIP switch; can be set to 'pull-up', 'pull-down' or 'float'
S5	USER-PB-SW5	On-board Push-button switch connected to SW5 input to FPGA
S6	USER-PB-SW4	On-board Push-button switch connected to SW4 input to FPGA
S7	FPGA-CONFIG	Push button switch to force FPGA to re-load its configuration
S8	RESET	On-board Push-button switch to force RESET
S9	USER-DIP	Front panel 4 pole DIP switch for User-Defined functions
S10	FPGA-CONFIG-MODE	Board mounted SMD 4 pole switch to set FPGA configuration mode and pull up mode

Table 4-4: List and definition of Switches

4.3 List of Jumpers

Name	Function	Type	Description
JP1	CAN-TERM1	2x2 pin header 0.1”	CAN bus termination – see section 2.9.1
JP2	CAN-TERM2	2x2 pin header 0.1”	CAN bus termination – see section 2.9.1
JP3	1553-TERM	2x2 pin header 0.1”	1553 bus termination – see section 2.11
JP4	USER-PB1	2 pin header 0.1”	For external/front-panel USER push-button
JP5	USER-PB2	2 pin header 0.1”	For external/front-panel USER push-button
JP6	RESET-PB	2 pin header 0.1”	For external/front-panel RESET push-button
JP7	VP-VN	2 pin header 0.1”	Accesses FPGA VP/VN ADC input
JP8	PROM-WP	2 pin header 0.1”	Install to protect FLASH PROM U12 from being written
JP9	PCI-M66EN	2 pin header 0.1”	Configures PCI to force 33MHz mode - §2.5
JP10	PCI-RSTN	3 pin header 0.1”	Configures RESET source
JP11	PCI-HOST	2x10 pin header 0.1”	Configures PCI pull-ups in host/peripheral mode - §2.5
JP12	PCI_CLK	2x2 pin header 0.1”	Configures PCI-CLK in host/peripheral mode - §2.5
JP13	PCI-ARB-REQ	4 pin header 0.1”	Configures PCI-arbiter in host/peripheral mode - §2.5
JP14	PCI-ARB-GNT	4 pin header 0.1”	Configures PCI-arbiter in host/peripheral mode - §2.5

Table 4-5: List and definition of PCB Jumpers

(for details refer to schematic, RD 1)

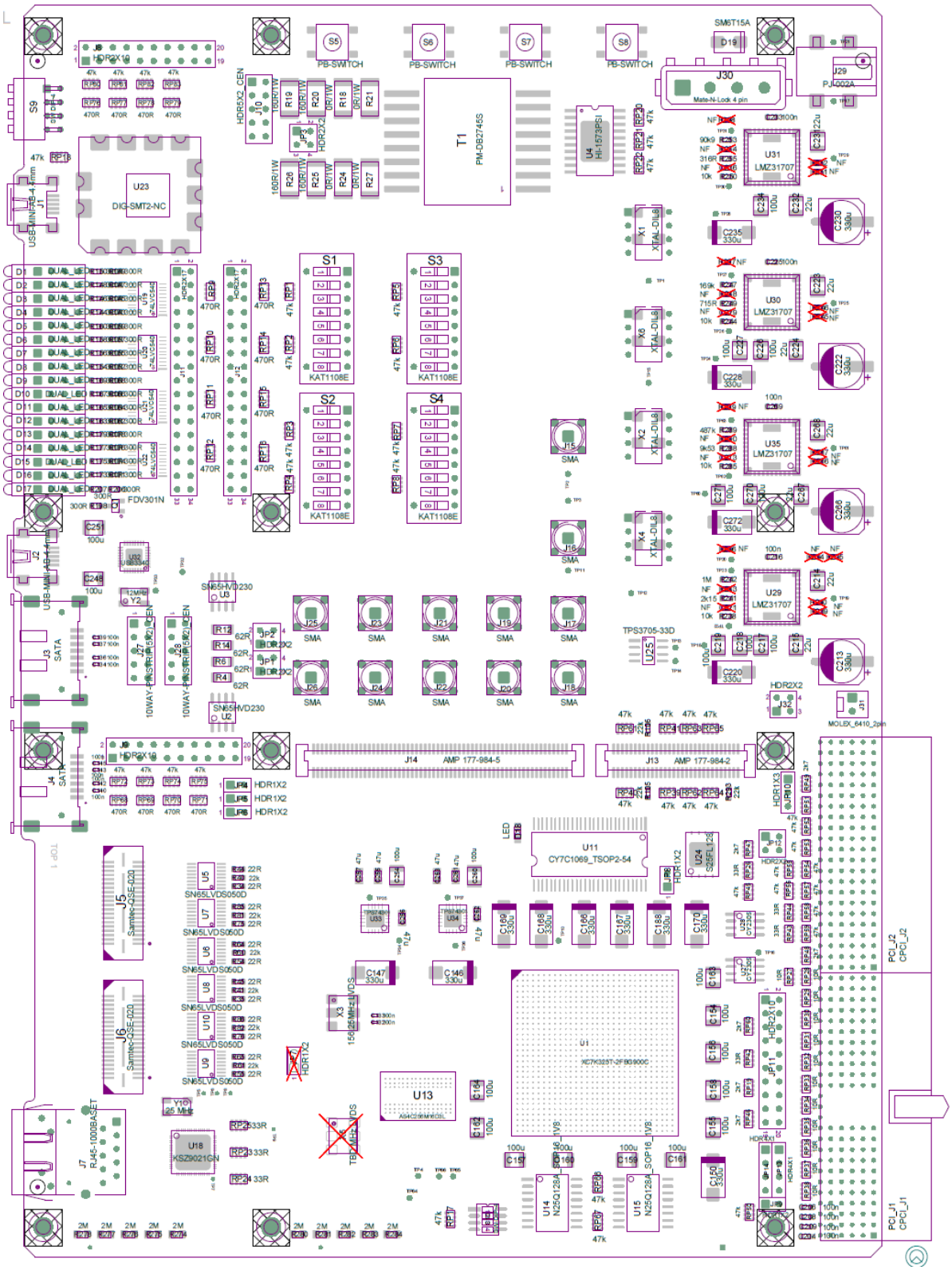

Figure 4-2: PCB Top View

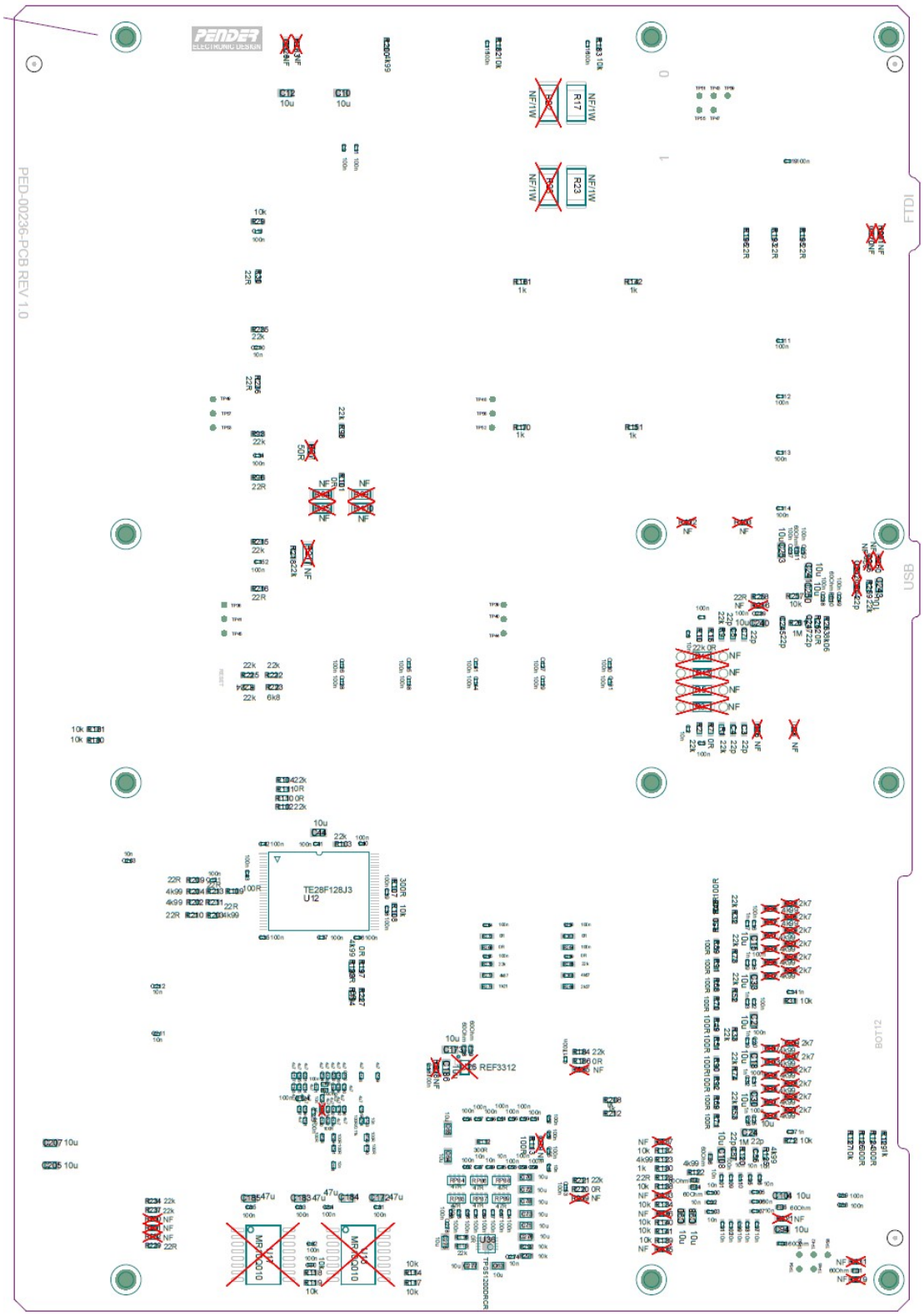

Figure 4-3: PCB Bottom View

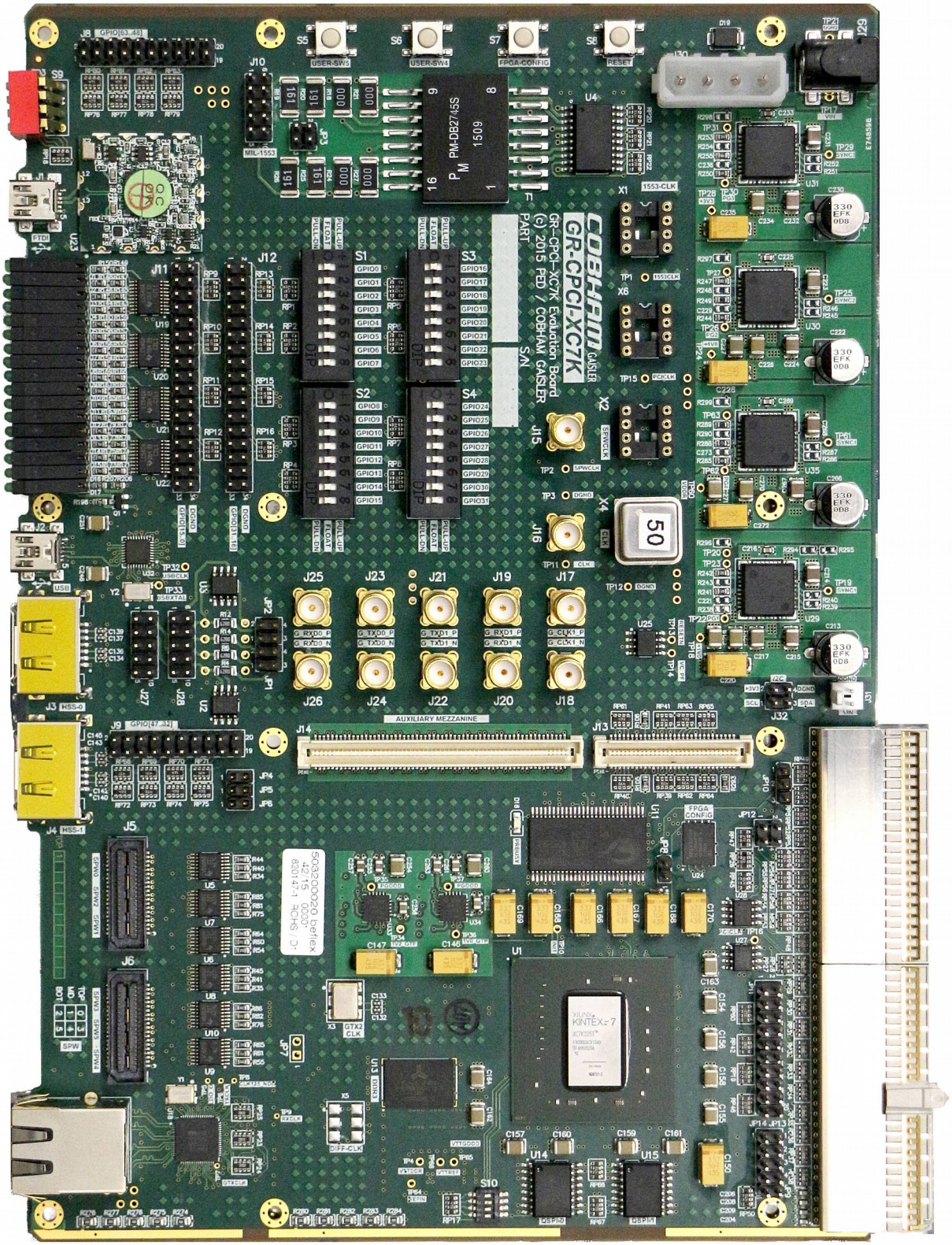

Figure 4-4: PCB Top View (Photo)

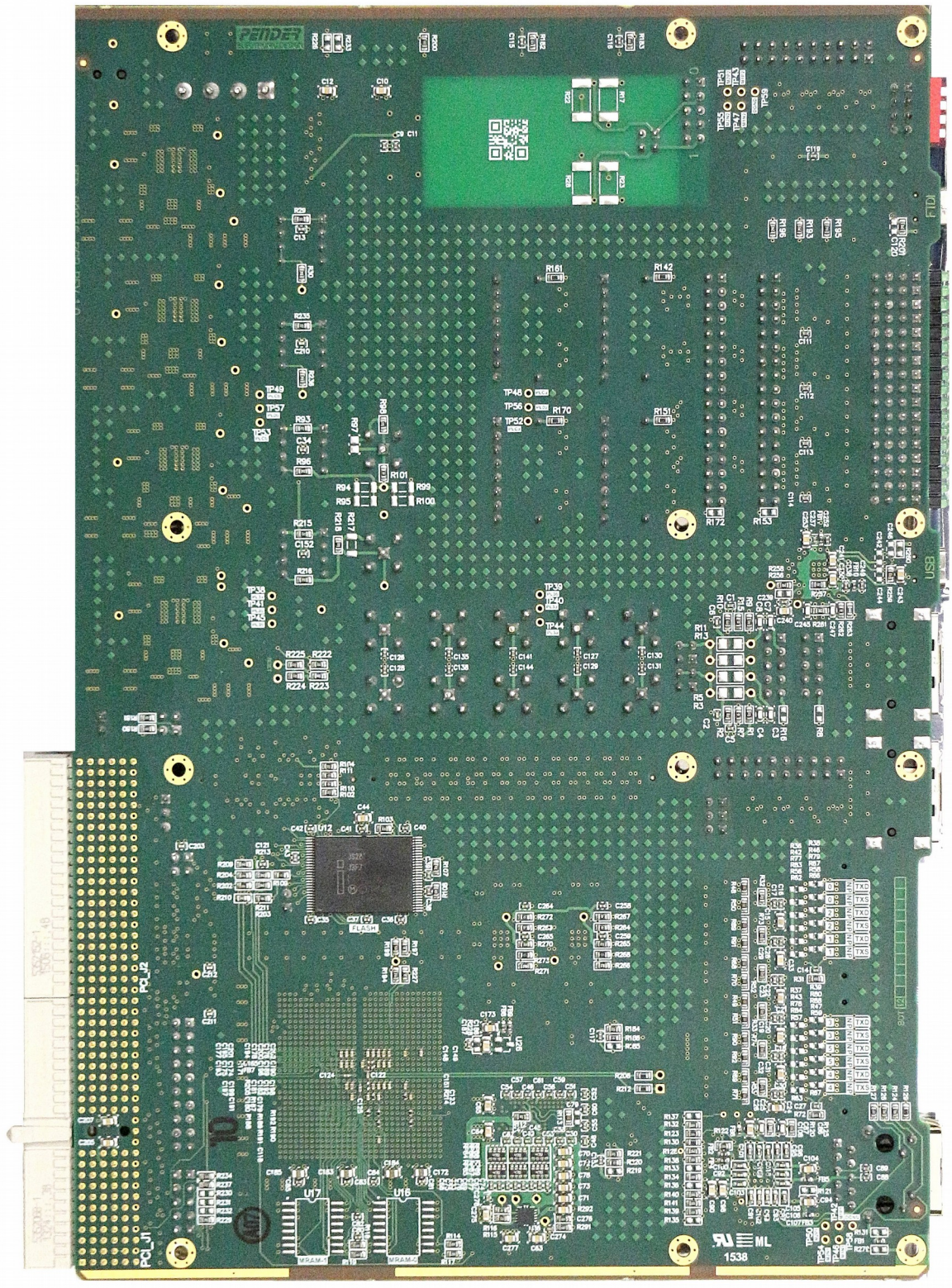

Figure 4-5: PCB Bottom View (Photo)