Memory Compatibility with FTMCTRL Memory Controller

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1 INTRODUCTION

1.1 Scope of the Document

This document describes compatibility of various SRAM, MRAM and PROM memories with the Aeroflex Gaisler's Fault-Tolerant Memory Controller (FTMCTRL) IP core, available in products such as GR712RC, UT699, UT699E, UT700 products and the GRLIB distributions.

The FTMCTRL has been subject to feature improvements over time. In this document features added to the memory controller in various product are addressed, and their impact on compatibility with various memory parts is described. The aim of this document is to provide an overview of known conditions where the various revisions of the FTMCTRL no longer meet the requirements of various memory parts. Worst case timing analysis shall always be performed to ensure compatibility for a particular design.

2 ABBREVIATIONS

TBC	To Be Confirmed
TBD	To Be Defined

3 OVERVIEW

The evolution of the FTMCTRL has been ongoing over several product generations in order to adapt to new timing requirement of memories. The IP core version implemented in the UT699 is oldest version considered in this document and is used as a baseline to compare against. The additional features that have been added to the FTMCTRL at major product releases are listed in the table below.

Product	**Feature Introduced**
UT699 GRLIB build ID: 2564	(Baseline)
GR712 GRLIB build ID: 3696	No changes for SRAM and PROM compatibility in relation with UT699
	Pipelined Reed-Solomon EDAC for SDRAM area. *The IP-core feature is enabled in the design by setting the "edac" VHDL generic to 3.*
UT699E and UT700 GRLIB build ID: 4110	One additional Lead Out cycle is added for PROM area write accesses to the already existing single lead out cycle. It holds the address bus stable for one more cycle while chip select and write enable are de-asserted. The additional Lead Out cycle is only added for the last write access performed on the memory bus if a burst write was performed on it. Thus when a 8 bit wide memory data bus is used a 32 bit AMBA write access will result in that the Lead Out cycle is applied on the last 8 bit write of four to the memory bus. *The IP-core feature is enabled in the design by setting the "rahold" VHDL generic to 1.*
	Pipelined Reed-Solomon EDAC for SDRAM area
GR740 GRLIB build ID: 4152	The additional Lead Out cycle feature introduced in the UT699E and UT700 is extended to allow the number of lead out cycles to be configurable through the APB registers of the FTMCTRL. The Lead Out cycle is applied to all write accesses performed on the memory bus including burst writes accesses. Another lead out functionality change done is that the data bus is also driven throughout the duration of the lead out. *The "rahold" VHDL generic is deprecated making the feature always included in the Lead Out design.*
	Added time out counter for the memory bus ready signal to prevent indefinite memory bus accesses.
	(The FTMCTRL SRAM area is not used in the design)

Table 1: FTMCTRL feature additions starting at UT699

The GRLIB build ID is listed in order to provide an approximate reference when a FTMCTRL feature was released in the GRLIB distribution. Note that for other products and RTAX designs the build ID is not an indicator that a certain FTMCTRL version or feature set is implemented (the FTMCTRL IP core is configurable at implementation time via several parameters – VHDL generics).

3.1 Lead Out Feature

The FTMCTRL lead out cycle(s) covers several memory timing constrains. In particular it may satisfy the following memory part requirements:

- Memory write recovery – time period before the memory is available for a new write operation after the previous write operation ended.
- Address hold timing – time that the address must be held stable after release of write strobe.
- Data hold timing – time that the data must be held stable after release of write strobe. (added in GR740)

4 MEMORY COMPATIBILITY

In the table below the compatibility for each memory part is described with various LEON devices. In the analysis column the memory part background is presented and the expected level of compatibility it has with a system.

Not all the requirements of each memory part are addressed here. Primarily timing requirements are presented and analysed that are deemed to be the most incompatible with various configurations of the FTMCTRL in the previously mentioned LEON systems. The analysis is performed assuming ideal circumstances where neither pad, buffer or propagation delays are considered, except those defined in the data sheet of the memory parts. Neither are any considerations taken into account when multiple memory parts co exist on the same memory bus.

Always refer to the latest memory part data sheet for the current specification.

Memory Part	Timing Characteristics	Analysis
UT8MR2M8 16Megabit Non-Volatile MRAM	Read time: 45 ns Write time: 45 ns Write recovery time (address hold): 16 ns	The memory requires a 16 ns address hold (lead out) time for write accesses after write strobe has been de-asserted. The system clock may therefore not exceed 62.5Mhz when only one lead out cycle is guaranteed. During write burst FTMCTRL inserts exactly two IDLE clock cycles after each write on memory bus. • 1st cycle releases write-strobe and chip enable • 2nd cycle increments the address and asserts CE • 3rd cycle asserts write-strobe for next write. **UT699 and GR712:** Not compatible above 62.5MHz since the FTMCTRL only holds the address stable one cycle after write strobe is released. **UT699E and UT700:** Not compatible above 125MHz since the address is only held stable during the two lead out cycles. These are only performed if the AMBA write access is made to the PROM area of the FTMCTRL, and requires that the accesses does not generate a burst write on the memory bus. Otherwise, if a sequential write is performed on the memory bus or the MRAM is placed on the SRAM area of the FTMCTRL behaves as in the UT699 and GR712, which limits system frequency to 62.5 MHz. **GR740:** No known incompatibility. The address hold during writes can be satisfied by using the configurable Lead Out feature. NOTE that the memory drives the data bus up to 10 ns after output enable is disabled for read accesses. Bus contention will occur for system frequencies above 200 MHz when read is followed by a write. This is because the FTMCTRL only guarantees two cycles between de-asserting the output enable in a read access until driving write data for a write access. **Data sheet date:** March 2015 **Doc no:**36-00-01-000 Ver. 1.0.0

Memory Part	Timing Characteristics	Analysis
UT8MR8M8 64Megabit Non-Volatile MRAM	Read time: 50 ns – Write time: 50ns Write recovery time (address hold): 16 ns	Same as UT8MR2M8 16Megabit above. **UT699 and GR712:** Not compatible above 62.5MHz since the FTMCTRL only performs one lead out cycles and therefore only holds the address stable for one cycle after write strobe is released. **UT699E and UT700:** Not compatible above 125MHz since the address is only held stable during the two lead out cycles. These are only performed if the AMBA write access is made to the PROM area of the FTMCTRL, and requires that the accesses does not generate a burst write on the memory bus. Otherwise, if a sequential write is performed on the memory bus or the MRAM is placed on the SRAM area of the FTMCTRL behaves as in the UT699 and GR712, which limits system frequency to 62.5 MHz. **GR740:** No known incompatibility. The address hold during writes can be satisfied by using the configurable Lead Out feature. NOTE that the memory drives the data bus up to 10 ns after output enable is disabled for read accesses. Bus contention will occur for system frequencies above 200 MHz when read is followed by a write. This is because the FTMCTRL only guarantees two cycles between de-asserting the output enable in a read access until driving write data for a write access. **Data sheet date:** March 2015 **Doc no:** 36-00-01-002 7 Ver. 1.0.0

Memory Part	Timing Characteristics	Analysis
UT8QNF8M8 64Mbit NOR Flash Memory	Read time: 60 ns Output enable release to High-Z: 16 ns – Write time: 60 ns Write pulse width high: 25 ns	The PROM operates in either 8 or 16 bit mode. It does not require specific data or address hold, but requires that the pulse controlling the write is de-asserted for 25ns between write accesses. The FTMCTRL performs write strobe controlled write accesses. Analysis of this requirement does not consider that software control could satisfy this requirement. NOTE that the data-bus turn off time is 16 ns long. The FTMCTRL only guarantees two cycles between de-asserting the output enable after a read access until driving write data for a write access. Bus contention may occur if clock period less than 16ns/2=8ns (125MHz). **UT699 and GR712:** Not compatible above 80 MHz, because of write pulse width high timing requirement. The FTMCTRL releases the write strobe for 2 cycles between each sequential write access PROM area. The fastest clock cycle period allowed is therefore 25ns/2=12.5ns (80MHz), without requiring additional lead out cycles. **UT699E and UT700:** Not compatible above 120MHz since the FTMCTRL will only de-assert the write-strobe for 3 cycles between consecutive write accesses, and thus the clock period is limed to 25ns/3=8.33 ns (120MHz). NOTE that this is valid when single write transfers are performed on the AMBA bus that do not exceed the width of the PROM memory bus. Otherwise if write bust accesses are performed the on the memory bus the write strobe is only de-asserted for a minimum of two cycles. This is the same behaviour as for UT699 and GR712 (80MHz). **GR740:** No known incompatibility. The write strobe de-assertment requirement after write accesses can be satisfied by using the configurable Lead Out feature. **Data sheet date:** September 9, 2013
UT8R512K8 512K x 8 SRAM	Read time: 15ns – Write time: 15ns Write address hold time: 2 ns Write data hold time: 2 ns	The chip requires both the active high and active low chip enable signals to be driven, and therefore requires an external inverter on PCB to accomplish this. **UT699, GR712, UT699E and UT700:** No known incompatibility, but requires an inverter externally on PCB to generate active high chip enable. Note: 2 ns data bus hold for write access has to be added externally. **Data sheet date:** March 2009

Memory Part	Timing Characteristics	Analysis
UT8ER512K32 Monolithic 16M SRAM MASTER	Read time: 20 ns – Write time: 10ns Write data hold time: 2 ns	The chip requires both the active high and active low chip enable signals to be driven, and therefore requires an external inverter on PCB. The on chip EDAC is enabled by default which requires the busy signal to be handled by the FTMCTRL. **UT699, GR712, UT699E and UT700:** Partially compatible with the EDAC functionality. Polarity of the scrub busy signalling of the SRAM does not match with the FTMCTRL and therefore an external inverter is required to correct the polarity. It is not possible to configure the EDAC function as the FTMCTRL can not leave chip enable signal asserted throughout the duration of the EDAC configuration sequence. The MBE (Multi Bit Error) pin has incompatible polarity with the BEXCN signal of the FTMCTRL. The MBE could be connected to GPIO instead and handled via interrupt. **Custom FTMCTRL:** Can be made compatible if custom designed. **Note:** Write Data hold of 2 ns has to be added externally. Both CE# and CE on this SRAM have to be connected. **Data sheet date:** July 24, 2012
UT8R128K32 128K x 32 SRAM	Read time: 15 ns – Write time: 15 ns Write data hold time: 2 ns	**UT699, GR712, UT699E and UT700:** No known incompatibility **Note:** Write Data hold of 2 ns has to be added externally **Data sheet date:** March 2009
QCOTS UT7Q512 512K x 8 SRAM	Read time: 100 ns – Write time: 100 ns	**UT699, GR712, UT699E and UT700:** Limited to 50 MHz if placed on SRAM interface of FTMCTRL since number of wait-states limited to maximum of 4 in total.
UT8Q512E 512K x 8 RadTol SRAM	Read time: 20 ns – Write time: 20 ns Write data hold time: 2 ns	**UT699, GR712, UT699E and UT700:** No known incompatibility. **Note:** Write Data hold of 2 ns has to be added externally **Data sheet date:** November 11, 2008
UT9Q512E 512K x 8 RadTol SRAM	Read time: 20 ns – Write time: 20 ns Write data hold time: 2 ns	Same as UT8Q512E 512K x 8 above **UT699, GR712, UT699E and UT700:** No known incompatibility. **Data sheet date:** Data Sheet September, 2008

Memory Part	Timing Characteristics	Analysis
UT7C138/139 4Kx8/9 Radiation-Hardened Dual-Port Static RAM with Busy Flag	Read time: 45/55 ns – Write time: 45/55 ns	The BUSY# signal is used to prevent address contention between the two ports. Polarity of the BUSY signal is not compatible with FTMCTRL. **UT699, GR712, UT699E and UT700:** No known incompatibility. Inverter is needed for the BUSY signal on PCB as polarity mismatch. **Data sheet date:** January 2002
UT8ER1M32 UT8ER2M32 UT8ER4M32 32/64/128 Megabit SRAM MCM	Read time: 20/22/25 ns Read Address to EDAC error flag valid: 22/22/25 ns – Write time: 10 ns	EDAC is enabled by default on memory. **UT699, GR712, UT699E and UT700:** Same on chip EDAC compatibility issues as with the UT8ER512K32. **Custom FTMCTRL:** Can be made compatible with EDAC feature. **Data sheet date:** June 2015 **Doc no:** 36-00-01-009 Version 1.0.0
UT8R1M39 UT8R2M39 UT8R4M39 40/80/160 Megabit SRAM MCM	Read time: 20/22/25 ns – Write time: 10ns	**UT699, GR712, UT699E and UT700:** No known incompatibility. **Data sheet date:** June 2015 **Doc no:** 36-00-01-008 Version 1.0.0
UT8Q512K32E 16 Megabit RadTolerant SRAM MCM	Read time: 25 ns – Write time: 25 ns Write data hold time: 2 ns	**UT699, GR712, UT699E and UT700:** No known incompatibility. **Note:** Write Data hold of 2 ns has to be added externally **Data sheet date:** Data Sheet June 28, 2011
UT9Q512K32E 16 Megabit RadTolerant SRAM MCM	Read time: 25 ns – Write time: 25 ns Write data hold time: 2 ns	**UT699, GR712, UT699E and UT700:** No known incompatibility. **Note:** Write Data hold of 2 ns has to be added externally **Data sheet date:** Data Sheet June 28, 2011

Table 1 FTMCTRL together with Aeroflex Memory