FRONTGRADE Gaisler

USER'S MANUAL

GR740-MINI Board User's Manual

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1 INTRODUCTION

1.1 Purpose and Scope of the Document

This document provides a User's Manual and interface document for the *GR740-MINI* development board.

The work has been performed at Frontgrade Gaisler AB, Gothenburg, Sweden.

1.2 Reference Documents

The following documents are referred as they contain relevant information:

[RD1] GR740MINI-QSG.pdf, Quick Start Guide, available from https://www.gaisler.com/gr740-mini

[RD2] "GR740 user manual and data sheet", available from https://www.gaisler.com/GR740

[RD3] GRMON3 User Manual, available from https://www.gaisler.com/GRMON3

[RD4] "CertusPro-NX Family, Data Sheet", Document number: FPGA-DS-02086 available from https://www.latticesemi.com

[RD5] "sysCONFIG User Guide for Nexus Platform, Technical Note", Document number: FPGA-TN-02099-2.5, available from https://www.latticesemi.com/

[RD6] "CertusPro-NX High-Speed I/O Interface, Technical Note", Document number: FPGA-TN-02244-1.1, available from https://www.latticesemi.com/

2 ABBREVIATIONS

AHB	Advanced High-performance bus, part of [AMBA]
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus, part of [AMBA]
DDR3	Double Data Rate
DSU	Debug Support Unit
EDAC	Error Detection and Correction
ESD	Electro-Static Discharge
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Logic Array
FTDI	Future Technology Devices International
GMII	Gigibit Media Independent Interface
GPIO	General Purpose Input / Output
HCSL	High speed Current Steering Logic
HPC	High Pin Count
I^2C	Inter-Integrated Circuit
IP	Intellectual Property
JTAG	Joint Test Action Group
LPC	Low Pin Count
LVDS	Low-Voltage Differential Signaling
MII	Media Independent Interface
SDRAM	Random Access Memory
SPI	Serial Peripheral Interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PHY	Physical Layer Device
PLL	Phase Locked Loop
PROM	Programmable Read Only Memory
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

3 GR740-MINI-BOARD DESIGN

3.1 Overview

This document describes the design and implementation of the *GR740-MINI* board. There is also a Quick Start Guide [RD1] available, describing used commands and syntax etc. for debugging and development.

The *GR740-MINI* board is a compact evaluation platform built around the Frontgrade GR740 quad-core LEON4FT SPARC V8 processor and Lattice Semiconductor FPGA CertusPro-NX. The board is designed with multiple electrical functions and interfaces with gives the user a flexibility to interact with the board.

Figure 3-1 GR740-MINI Development board

The board contains the following main items.

- 2 x USB-C connectors for debug and power
- GR470 Processor
  - 1 x USB interface via *FTDI FT4232* providing JTAG and UART
  - 1 x Ethernet for communication and debug
  - 4 x SpaceWire channels to FMC+ connector
  - 256MB SDRAM
  - 128MB FLASH
- CertusPro-NX FPGA
  - 1 x USB interface via *FTDI FT4232* providing JTAG and UART
  - 1 x Ethernet for communication and debug
  - 4 x SerDes to FMC+ connector
  - LVDS to FMC+ connector
  - 3V3 IO to FMC+ connector
  - I^2C link to FMC+ connector
  - 1GB DDR3 memory
  - 512Mb SPI FLASH
- Intercommunication between GR740 and CertusPro-NX
  - PCI link (32bit, 33MHz)
  - GMII/MII
  - 4 x SpaceWire channels

3.2 Handling

ATTENTION: OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This unit contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the unit observe appropriate precautions and ESD safe practices.

When not in use, store the unit in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the unit is in an un-powered state.

When operating the board in a 'stand-alone' configuration, the power supply should be current limited to prevent damage to the board or power supply in the event of an overcurrent situation.

This equipment has SpaceWire ports that use Low Voltage Differential Signalling (LVDS) which has limited common mode voltage protection. To avoid damage to the SpaceWire interfaces due to common mode voltage see section 4.10 FMC+ connector

4 BOARD DESIGN

This section describes the board design in detail. The electrical functions and interfaces that are common for both the devices (the processor and the FPGA) are described in the first sections: 4.1 to 4.6. In section 4.7 and 4.8 each device and corresponding functions/interfaces are described. The intercommunication between the devices is described in section 4.9 and the FMC+ connector in section 4.10.

Note: This design is not aimed for flight and should not be used as a reference design.

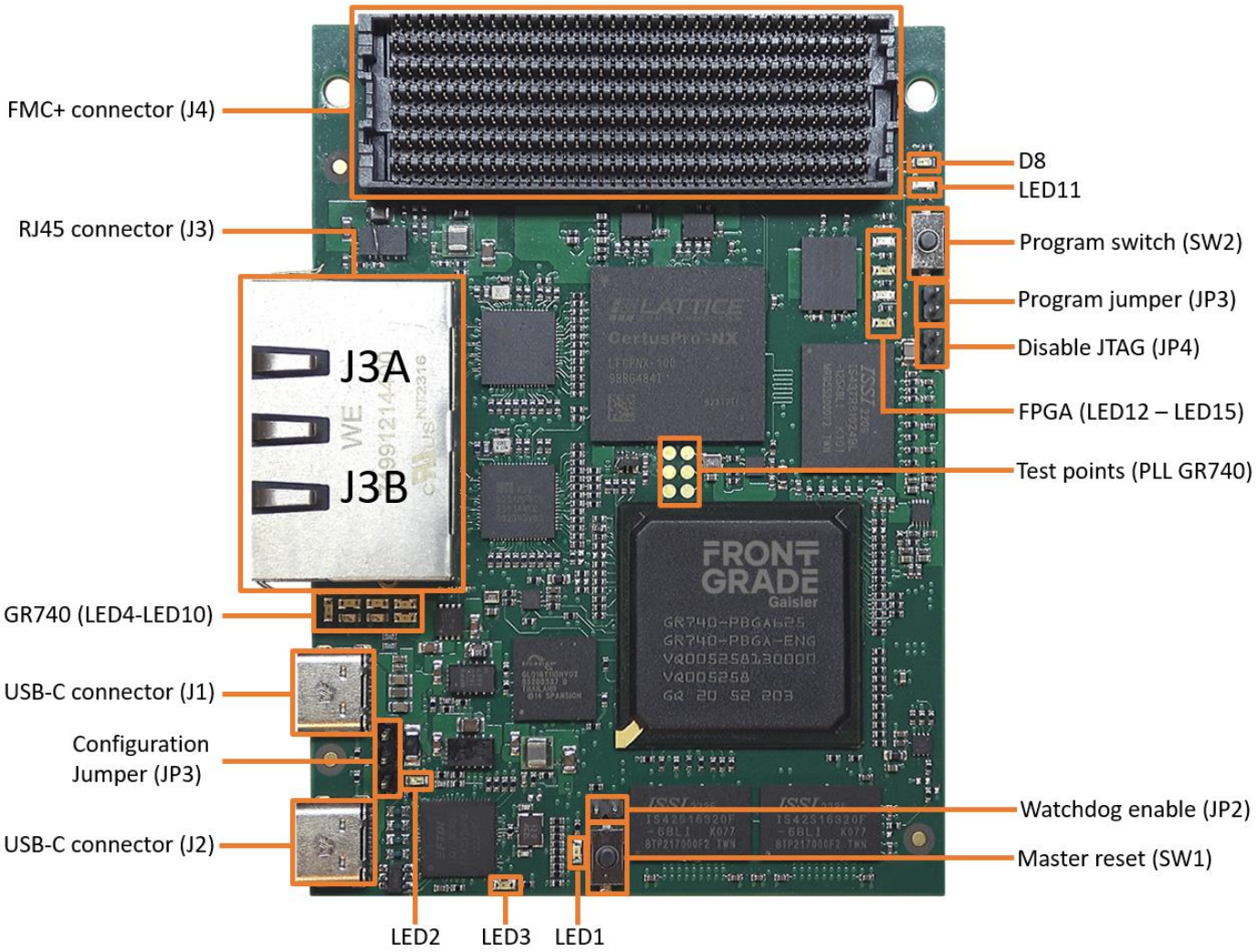

Figure 4-1 Top view of GR740-MINI board

Figure 4-1 shows the top view for the *GR740-MINI* board and is marked with interactions and indications. For a more detailed assembly drawing referring to Appendix A & B.

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4.1 Board block diagram

The *GR740-MINI* Development Board provides the electrical functions and interfaces as represented in the block diagram in Figure 4-2.

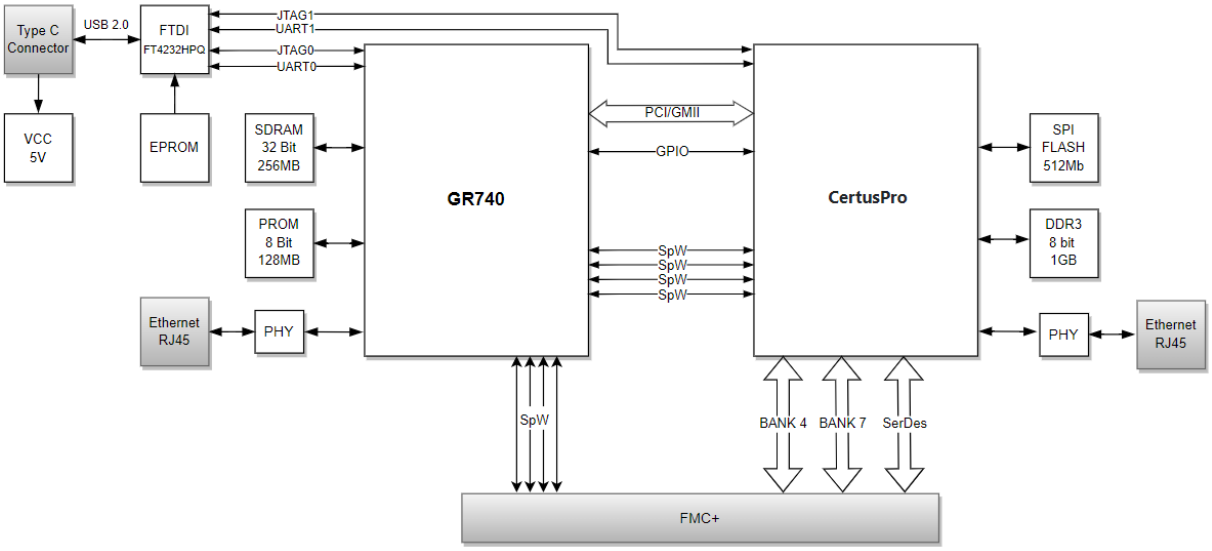

Figure 4-2 GR740-MINI Board block Diagram

There are multiple ways to communicate with the board, in Figure 4-2 the interfaces are represented as grey boxes and described shortly below.

1. **USB 2.0**: The USB 2.0 link is connected to a FTDI chip that converts the USB-data into four serial outputs (2 x JTAG and 2 x UART) connected to both the FPGA and Processor. USB 2.0 interface is connected to connector J2.

2. **Ethernet**: Both MII and GMII interface are supported by the FPGA and processor through J3.Where J3A is to CertusPro-NX and J3B to the GR740.

3. **FMC+ connector**: the usage of the FMC+ connector is dependent on an external mezzanine board. In this design the FMC+ connector provides the GR740 with four SpaceWire channels and the CertusPro-NX with SerDes LVDS, I^2C and GPIO 3V3.

4.2 Power the board

The GR740-MINI board is powered using either of the USB-C connectors (J1 or J2). Therefor there are two ways to power supply the board and which is accomplished by attaching a 2-pin jumper to the 3-pin head (JP5), see Figure 4-3

The overall power requirement for the board is 15W. J2 is considered as the main power supply, and the configuration jumper is set to this as default (JP5: 1-2). This can be used when communicating with USB-C (data and power through the same cable), Ethernet or FMC+ connector. The USB-C source must handle at least 3A, 5V (15W). J2 must be inserted to start up the board since the D_N/P signals are needed to the FTDI chip see Figure 4-3.

There is only one exception when there is need to use J1 as power source. This is when the user is communicating with USB and the USB-source (for example a computer or a docking station) cannot handle the power requirements. Then, the users need to have an external power source connected to J1 and the data to J2, this configuration is chosen when setting jumper in JP5: 2-3 mode.

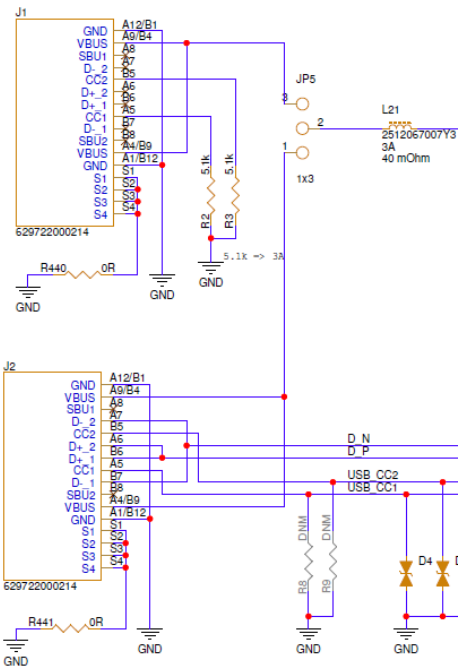

Figure 4-3 USB-C connector for power supply solution

Note: that the source (for example a computer, charger or docking station) used in this case must have a USB-C connector that can deliver **at least 3A, 5V (15W)**. Observe that not all sources with USB-C sockets support that. Check the sources manual before connecting to the *GR740-MINI* board.

4.3 Interacting with the board

As mentioned in section 4.2 there are two ways to power supply the board, by setting a configuration jumper. This configuration jumper is shown in Figure 4-4.

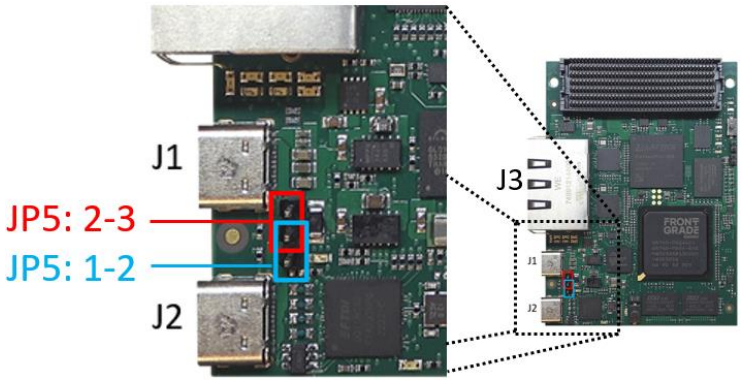

Figure 4-4 Jumper Configuration

On the board there are three LED for indicating power availability and communication status, see Table 4-1 for more information and Figure 4-5 for the board placement.

Table 4-1 Power and status LED

LED	Colour	Comment
LED1	Green	Indicates that 3V3 is available
LED2	Red	Light when USB is in suspended mode
LED3	Green	Indicate normal operational mode.

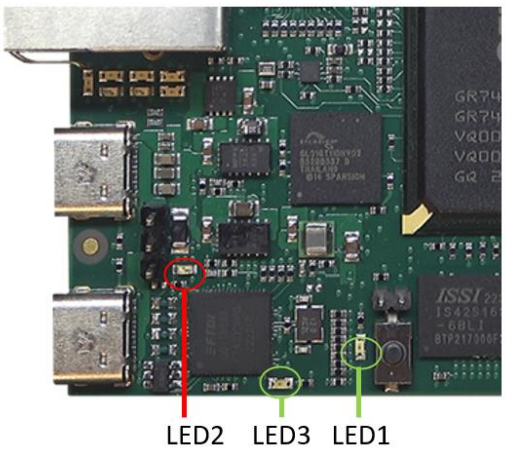

Figure 4-5 LED(1-3) board placement

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4.4 Power supplies

A block diagram showing the power supply design for the *GR740-MINI* board is shown in Figure 4-6. Since this board is power supplied through USB the FTDI chip that handles the communication via USB is powered up first via a dedicated voltage. A GPIO from the FTDI chip goes HIGH after the handshake is performed with OK result. This signal enables the rest of the power supplies through a voltage sequencer. The voltage sequencer (MAX16027TP+) will enable the different voltages in specific order with a fixed time delay set by an external capacitor. The enable signals are depending on the previous voltage supplies power-good (output) signal. The voltage sequence is designed to fulfil the power-up requirements for the GR740. The FPGA do not have any power up requirements and is enabled afterwards. Figure 4-7 shows the implementation for the voltage sequencer.

For most voltages switched point of load DC/DC converters are used. The type of DC/DC converters (LMZ21701, MPM3630 & MPM3620) are chosen because they are small, can supply the required currents and have integrated inductors. For the GR740 PLL voltage an ultra-low noise low drop out regulator (LDO) (TPS79601) is used

To achieve the right power setup to the DDR3 memory interface a dedicated DDR3 termination circuit (TPS51200) is used.

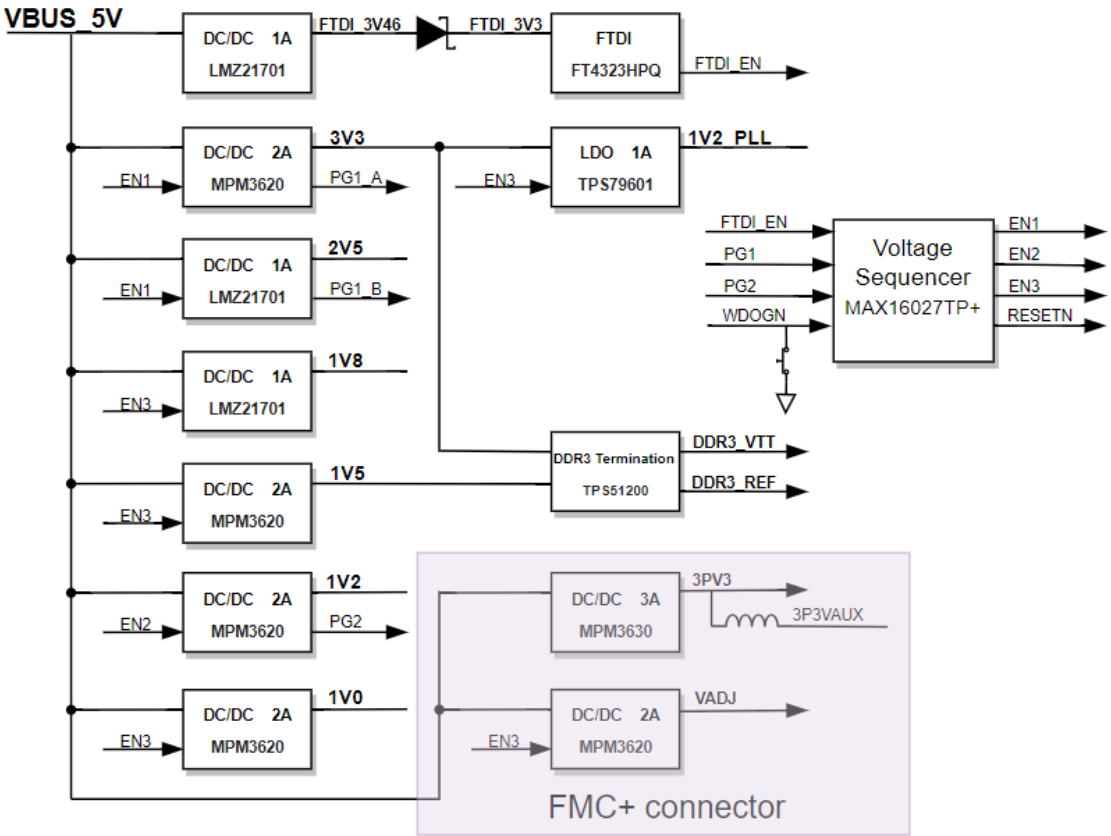

Figure 4-6 Power Regulation Scheme

Table 4-2 below list the different voltages for the GR740-MINI board with their main users.

Table 4-2 Voltages

Voltage	Main users
FTDI_3V46	FTDI chip, EPROM
FTDI_3V3	FTDI chip
3V3	Oscillator, Clock buffer, Processor (GR740), FLASH memory, SDRAM, Ethernet PHY, SPI FLASH, FPGA (CertusPro-NX)
3PV3	FMC+ Connector
3PV3AUX	FMC+ Connector
2V5	FPGA (CertusPro-NX), Processor (GR740)
1V8	FPGA (CertusPro-NX)
1V5	FPGA (CertusPro-NX), DDR3 Termination, DDR3 Memory
1V2	Ethernet PHY, Processor (GR740)
1V2_PLL	Processor (GR740)
1V0	FPGA (CertusPro-NX)
VADJ (1.8V)	FMC+ Connector , FPGA (CertusPro-NX)

4.5 FTDI chip

The *GR740-MINI* board provides Serial to USB interface chip, FT4232HPQ from FTDI, which provides up to 4 serial ports connect to a single USB-C connector (J2). The FTDI chip is connected to both the GR740 and the CertusPro-NX with JTAG and/or UART, see Table 4-3 for the port assignments. There is an EEPROM connected to the FTDI chip aimed for configuration. A separate 12 MHz crystal is dedicated for the FTDI chip. See the Quick Start Guide [RD1] for more information about usage.

Table 4-3 FTDI Port assignment

Port	Function	Target
A	JTAG	GR740
B	JTAG	CertusPro-NX
C	UART	GR740
D	UART	CertusPro-NX

4.6 Reset

The reset signal is active low and is connected to the processor GR740, FPGA CertusPro-NX, PROM memory, Ethernet PHY (GR740), Ethernet PHY (CertusPro-NX) and it is derived from the voltage sequencer. Figure 4-7 shows the implementation for the voltage sequencer. The reset signal is held low by the sequencer until all the enable (output) signals are high. The reset signal is controlled by a master-reset (input) signal. This signal is also active low and have a pull-up resistor connected to it. The watchdog signal from the GR740 is connected to the master-reset signal through a jumper, by default this is disabled, refer to section *4.7.5* for more information. There is also a switch (SW1) to the master-reset signal for manually reset the board, see Figure 4-1 for placement.

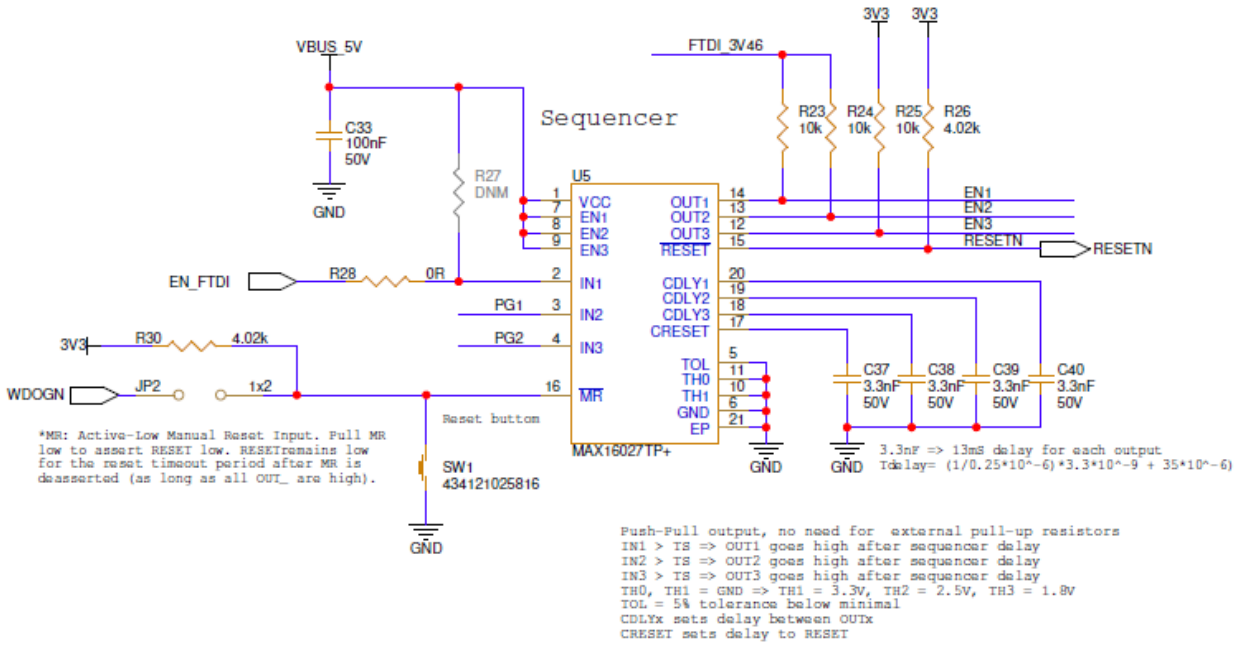

Figure 4-7 Implementation of voltage sequencer

4.7 GR740 Processor

The Frontgrade Gaisler GR740 processor is a radiation-hard system-on- chip featuring a quad-core fault-tolerant LEON4 SPARC V8 processor, and a set of IP cores connected through AMBA AHB/APB buses as represented in the Figure 4-8.

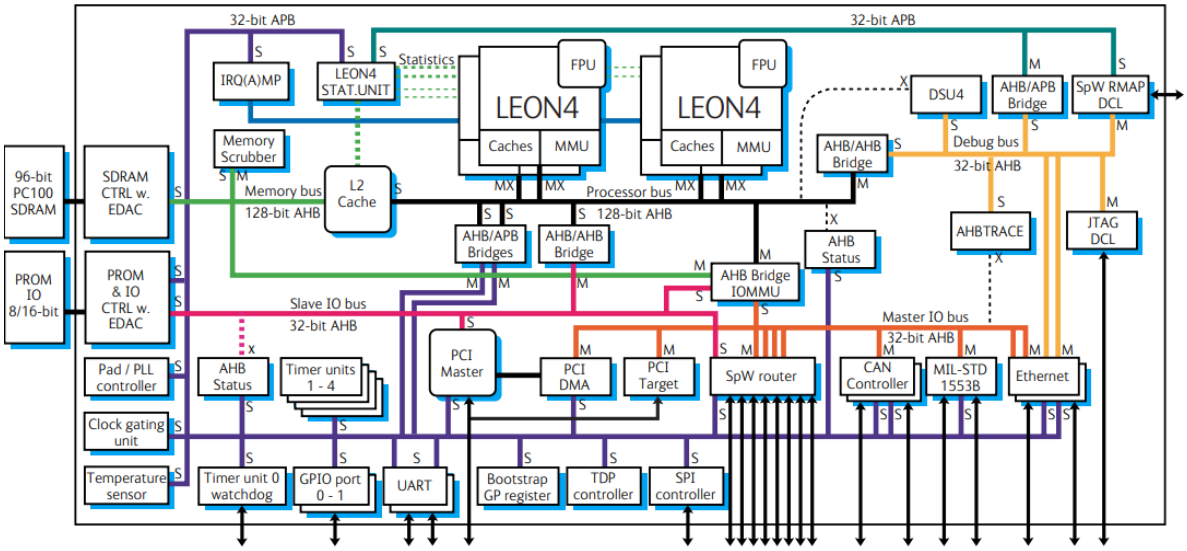

Figure 4-8 GR740 SOC Block Diagram

The details for the interfaces, operation, and programming of the GR740 processor are given in [RD2].

This GR740 processor is packaged in a 625-pin, 1mm pitch plastic Ball Grid Array package (27 x 27 mm).

Figure 4-9 GR740 Package

4.7.1 Bootstrap signals

The power-up and initialisation state for the GR740 is affected by several external signals. A number of GPIO:s and function pins are predefined for this purpose. To set the desired setting a pull-up or pull-down resistors are used to set the signal to HIGH or LOW. For more detailed information about the bootstrap signals see section 3.1 in GR740 User Manual [RD2].

As shown in Figure 4-10 there are options to change most of the bootstrap values since there are additional not mounted resistors in the schematic.

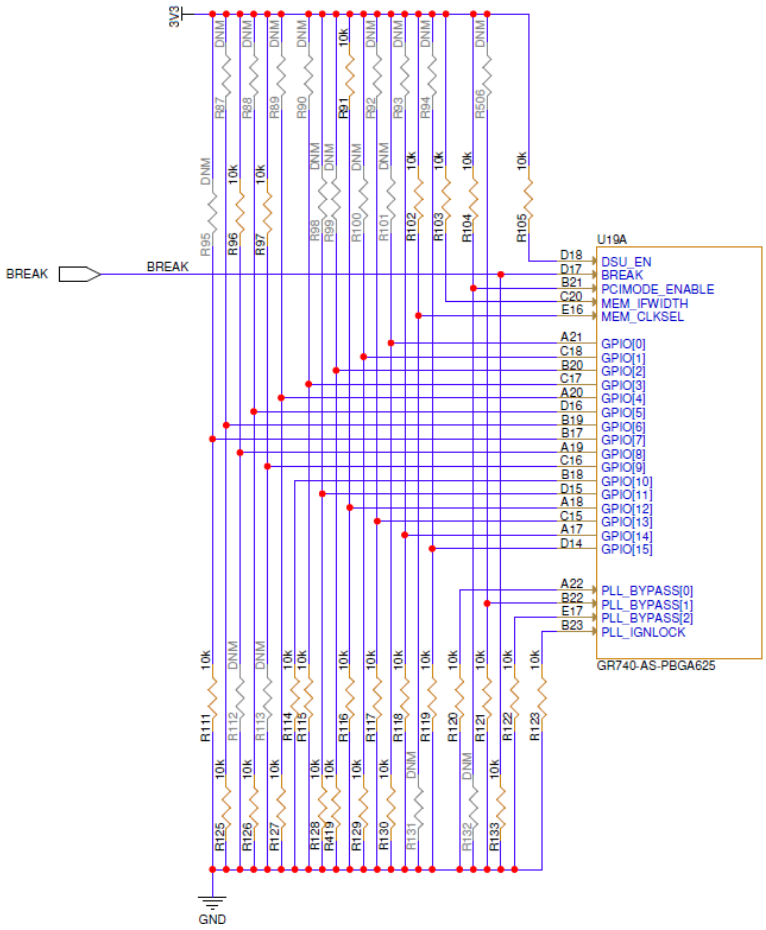

Figure 4-10 Bootstrap signals

The default configuration for those signals in the GR740-MINI design is shown in Table 4 3.

Table 4-4 Default bootstrap values

Bootstrap signal	Pin	Default	Description
DSU_EN	D18	HIGH	Enables the Debug Support Unit (DSU)
BREAK	D17	LOW	Puts all processors in debug mode when asserted
PCIMODE_ENABLE	B21	HIGH	Enables PCI mode.
MEM_IFWIDTH	C20	HIGH	Selects the half width SDRAM interface
MEM_CLKSEL	E16	HIGH	Set external source to the memory clock.
GPIO[0]	A21	LOW	Sets the IP and MAC address for Ethernet Debug Communication Link.
GPIO[1]	C18	LOW	
GPIO[2]	B20	LOW	
GPIO[3]	C17	LOW	
GPIO[4]	A20	LOW	
GPIO[5]	D16	LOW	
GPIO[6]	B19	LOW	Selects SpaceWire router Distributed Interrupt configuration: Interrupts with acknowledgment mode (32 interrupts with acknowledgments)
GPIO[7]	B17	LOW	
GPIO[8]	A19	HIGH	Ethernet Debug Communication Link routed over the Debug AHB bus
GPIO[9]	C16	HIGH	
GPIO[10]	B18	LOW	Selects the PROM width to 8-bit.
GPIO[11]	D15	LOW	The SpaceWire router is not disabled after reset
GPIO[12]	A18	LOW	Sets the two least significant bits of the SpaceWire router's instance ID.
GPIO[13]	C15	LOW	
GPIO[14]	A17	LOW	Disable EDAC of the PROM area
GPIO[15]	D14	LOW	Enables PROM/IO after reset
PLL_BYPASS[0]	A22	LOW	Bypass PLL and use clock input directly. 2: SpW clock, 1: SDRAM clock, 0: System clock PLL bypass.
PLL_BYPASS[1]	B22	LOW	
PLL_BYPASS[2]	E17	LOW	
PLL_IGNLOCK	B23	LOW	The PLL outputs of the device are gated until the PLL lock outputs have been asserted.

4.7.2 Debugging

In this design the debugging interfaces that are provided are JTAG and Ethernet (EDCL). Program download and debugging to the processor is performed using the GRMON3 Debug Monitor tool from Frontgrade Gaisler [RD3]. For more information about the debugging referring to the GRMON3 documentation [RD3] and the Quick Start Guide [RD1]

There are three debug control signals.

1. DSU_EN (input): This signal is a bootstrap signal which is pulled high on the board to enable debugging.

2. BREAK (input): This signal puts all processors in debug mode when asserted while DSU_EN is HIGH. On this board the signal is pull-down and connected to pin ADBUS7 on the FTDI chip, this feature allows GRMON to break the reset-loop by the flag -ftdigpio

3. DSU_ACTIVE (output): When the processor is halted.

4.7.3 LED

On the board there are LEDs corresponds to the GR740, see Table 4-5 for more information and Figure 4-11 for the board placement.

Table 4-5 LED correspond the GR740

LED	Colour	Comment
LED4	Green	Connected to DSU_ACTIVE, indicates when debug support unit is active.
LED5	Red	Connected to PROC_ERRORN signal, will indicate when processor 0 enters error mode.
LED6	Red	Connected to WDOGN, for more information see section 4.7.5
LED7	Green	Connected to GPIO2[5]
LED8	Green	Connected to GPIO2[6]
LED9	Green	Connected to GPIO2[7]
LED10	Green	Connected to GPIO2[8]

Figure 4-11 LED(4 -10) board placement

4.7.4 JTAG

GR740 supports JTAG interface for debugging. This link is accessible via J2 (USB-C) through the FTDI chip.

4.7.5 WDOGN

The GR740 processor includes a Watchdog timer function which can be used for the purpose of generating a system reset in the event of a software malfunction or crash. To utilise the Watchdog feature, it is necessary to appropriately set-up and enable the Watchdog timer. Please consult the GR740 processor User Manual [RD2] for the correct register locations and details. On this development board the WDOGN signal is connected to the master-resetn on the voltage sequencer via a jumper, see Figure 4-7. More information about the reset functionality refer to section *4.6.* By default, the jumper (JP2) is not installed so the watchdog timer function is disabled, to enable this function the jumper needs to be installed.

For software development it is often convenient or necessary to disable the Watchdog triggering to be able to easily debug without interference from the Watchdog operation. In this case, the jumper should not be installed. If the watchdog triggers when the jumper is **not** installed, no system reset will occur, but the Watchdog LED, LED6 will still illuminate.

4.7.6 Oscillators and clock input

Figure 4-12 shows the oscillator and clocks scheme for the GR740. For more details of the internal PLL structure, clock gating and multiplexing features of the GR740, see section 4 in the GR740 User Manual [RD2].

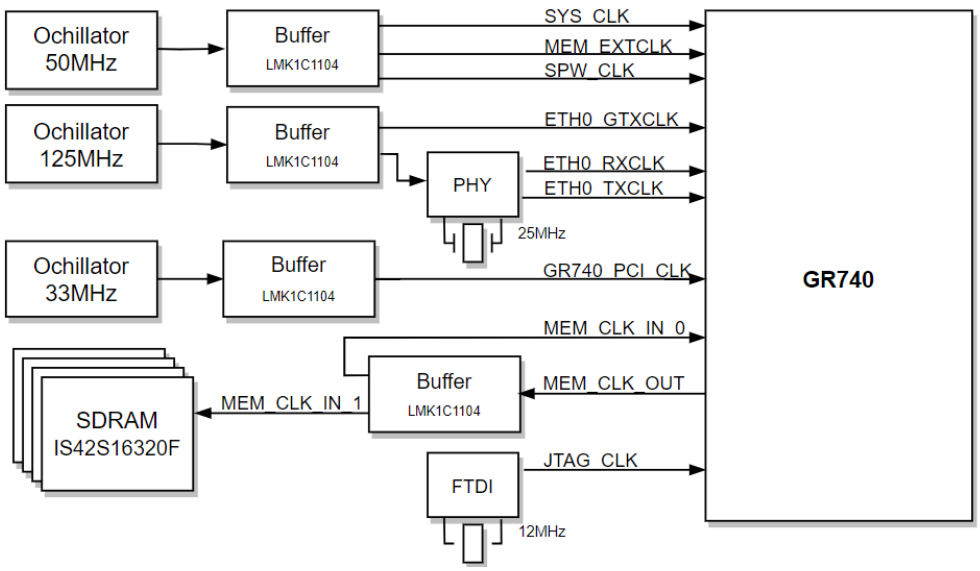

Figure 4-12 GR740 Clock Distribution *scheme*

The system clock (SYS_CLK), memory interface clock (MEM_EXTCLK) and the SpaceWire clock (SPW_CLK) are all separate inputs on the GR740 with a frequency of 50MHz. The signals originate from the same clock but are buffered through a high-performance, low-skew clock buffer (LMK1C1104) with separate outputs. The GR740_PCI_CLK originates from a 33MHz oscillator and is also buffered.

When Ethernet is in GMII mode the 125MHz clock is buffered (LMK1C1104) into the GR740 (ETH0_GTXCLK) and to the Ethernet PHY (transmit reference clock). Due to the output delay in the GR740 on transmitter clock the signals need to be a skewed from each other. Therefor the clock signal to the Ethernet PHY is delayed with 1ns in the layout. The Ethernet PHY also has a feature to skew the signal, and this can be used to tune the skewing. The ETH0_RXCLK frequency is 125MHz and is derived from the Ethernet PHY.

In MII mode the ETH0_GTXCLK is not used. The ETH0_RXCLK and ETH0_TXCLK frequency are 25MHz and derived from the Ethernet PHY.

The PHY uses an external crystal of 25MHz.

Due to limitations in the driving strength of the output clock signal MEM_CLK_OUT, this signal is needed to be externally buffered (LMK1C1104) to signal MEM_CLK_IN_0 and MEM_CLK_IN_1 back to itself as an input and to the SDRAM.

The JTAG_CLK is derived from the FTDI chip, which has an external crystal of 12MHz.

4.7.7 SDRAM

GR740 supports SDRAM in full-width (64 data bits) or half-width (32 data bits) mode. There is also a feature to add check bits (0, 8, 16 or 32) depending on the EDAC configuration. Since this design uses the PCI/ETH1 interface the SDRAM mode is limited to the half-width mode and with no EDAC due to shared pins. In this design the double chip select mode is used and therefor the flag -sddcs in GRMON must be set, see also [RD1], [RD2] and [RD3].

Four 512Mbit SDRAM (IS42S16320F-6BLI) as 32Mx16 has been combined in to one SDRAM with organization 64x32 with a total memory size of 256MB. Figure 4-13 shows the implementation for the SDRAM.

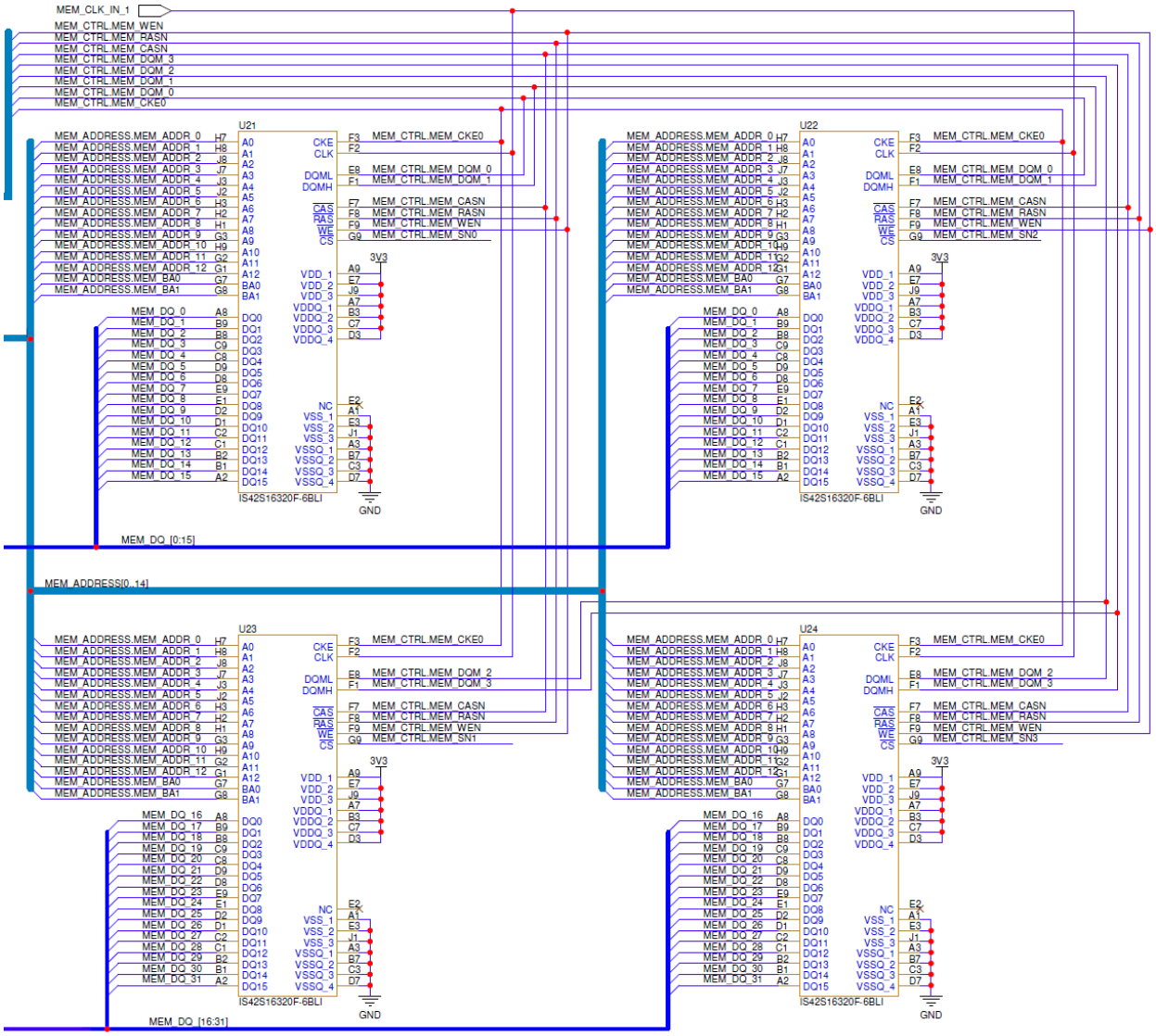

Figure 4-13 Implementation for SDRAM

4.7.8 PROM

GR740 supports PROM in 8- or 16-bit mode. However, since the design use UART0 (CTS signal is not used) the PROM mode is limited to 8-bit due to shared pins. The pins that will be occupied by UART0 are: PROMIO_DATA[7] and PROMIO_ADDR[27]. Therefor the upper 8 bit PROMIO_DATA[8:15] are used, and the ADDRESS positions are 0x0000 0000 – 0x07FF FFFF, with a data width of 8-bits in turn generates a maximum memory size to 128MB.

The PROM memory used in this design (S29GL01GT11DHV023) provides 128MB of Non-volatile storage organized as 128M x 8 operating.

This device can be used for program storage or as a boot device for the board.

The board is delivered with a pre-programmed boot memory, please see the Quick Start Guide [RD1] for more information.

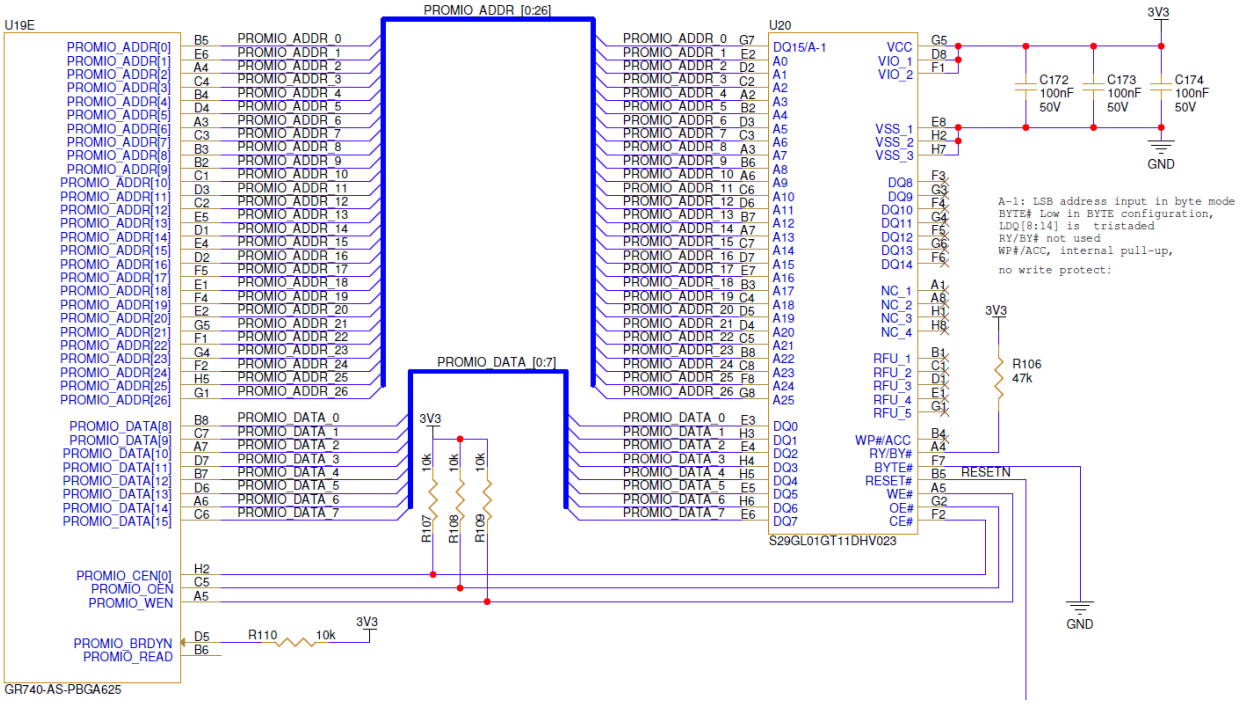

Figure 4-14 Implementation of PROM memory

4.7.9 Ethernet

The GR740 processor device incorporates two Ethernet controllers (ETH0 & ETH1) with support for GMII and MII interfaces. The *GR740-MINI* board provide a dual RJ45 connector (J3), with two corresponding Ethernet PHY transceivers, where one ethernet interface goes to the first ethernet controller (ETH0) on the GR740 and the other to the CertusPro-NX.

Figure 4-15 shows the implementation for the ETH0 interface. The RJ45 connector used has an integrated transformer. The ethernet PHY transceiver (KSZ9031) supports 10/100/1000Mbit/s Ethernet. The transceiver requires a dedicated 25MHz oscillator. It is different clock configuration depending on which ethernet mode that is used, se section *4.7.6* for more information. The management signals (ETH0_MDC, ETH0_MDIO and ETH0_MDINT) from the GR740 is connected both to its own PHY and to the FPGA. This feature allows the GR740 to control both PHY:s. If not used these signals must be set to high-Z in the FPGA design.

PHY address is hard-wired to 1 (“001”).

For more information on the registers and functionality of the Ethernet MAC+PHY device please refer to the data sheet for the KSZ9031 device

The default IP address for ETH0 : 192.168.0.24

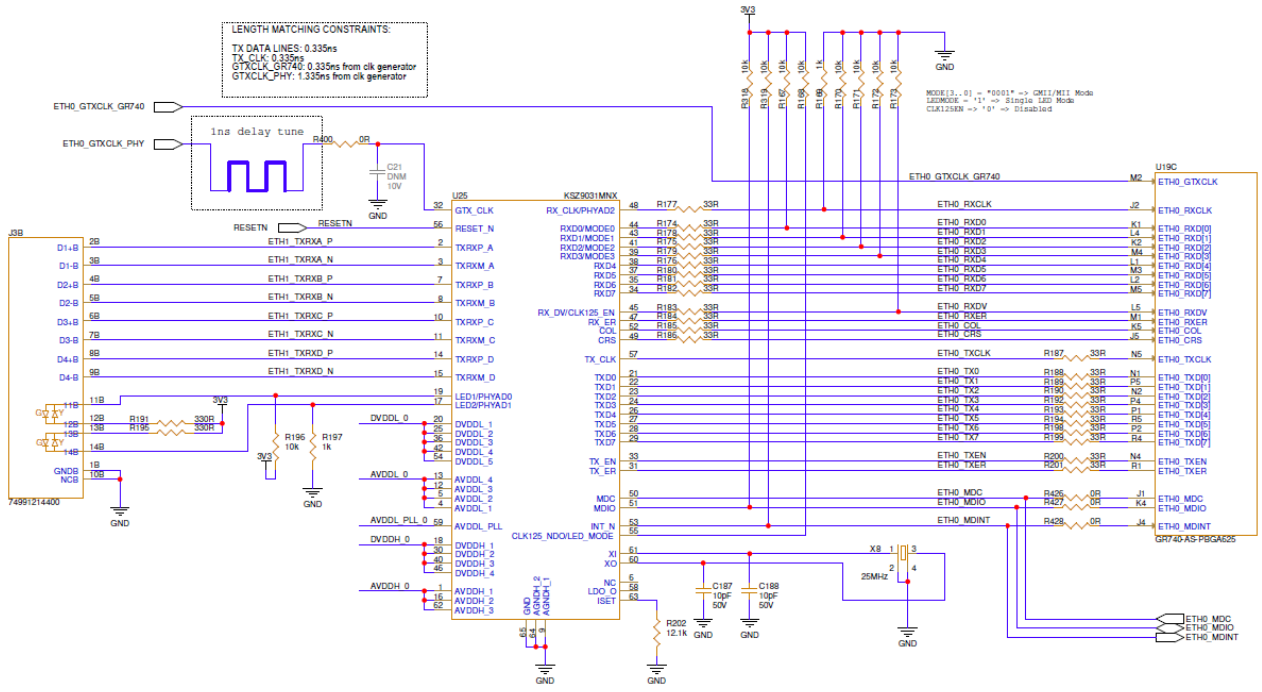

Figure 4-15 ETH0 implementation

The Ethernet interface can be used to communicate or to debug (EDCL) the GR740.

The ETH1 can be used as a intercommunication between the processor and the FPGA, see more in section *4.9.2 GMII*

4.7.10 SpaceWire

The GR740 provides a SpaceWire Router with 8 SpaceWire ports. Each SpaceWire interface consist of 4 LVDS pairs, 2 input pairs and 2 output pairs, *DATA IN*, *STROBE IN*, *DATA OUT*, *STROBE OUT*. SpaceWire ports [0:3] are connected to the FMC+ connector and ports [4:7] are connected to the FPGA see Figure 4-27. All the SpaceWire signals are routed in the PCB with an impedance of 100Ω. For more information about the implementation of SpaceWire refer to section *4.9.3* or *4.10*

4.7.11 GPIO

GR740 have some pins that are dedicated for GPIO. In this design GPIO2[0:4] is connected to the FPGA and there are resistors mounted in series to limit the current. GPIO2[5:8] is connected to green LEDs. See Figure 4-16.

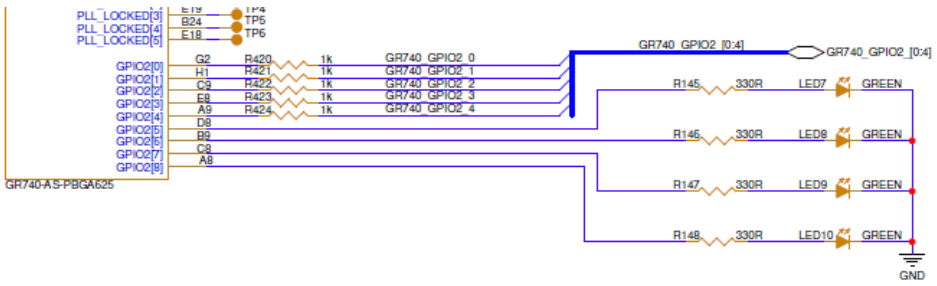

Figure 4-16 GPIO for GR740

4.8 CertusPro-NX FPGA

CertusPro-NX is a low-power general purpose FPGA and is built on the Lattice Nexus FPGA platform, using low-power 28 nm FD-SOI technology. In this design the LFCPNX-100-9BBG484 is used, which is the commercial-off-the-shelf (COTS) variant of the radiation-tolerant CertusPro-NX-RT FPGA. It provides a total of 100k logic cells and speed grade -9 (fastest) in a package size of 19x19mm, (ball-pitch of 0.8mm). For more information about the CertusPro-NX, see the corresponding data sheet [RD4].

The *GR740-MINI* board can be used to demonstrate features like SerDes, LVDS, Ethernet and the DDR3 DRAM interface for the CertusPro-NX see Figure 4-17.

Pre-developed bitstreams with Gaisler IP for download on the webpage https://www.gaisler.com/gr740-mini for plug-and-play and features for the *GR70-MINI* board are available.

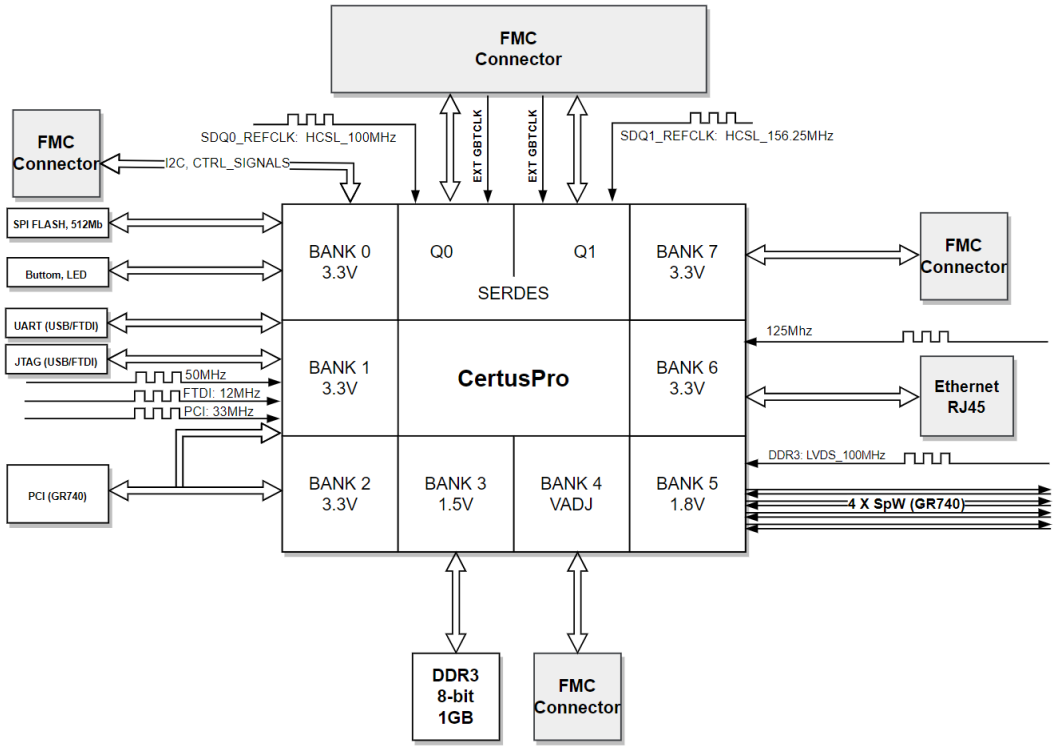

Figure 4-17 CertusPro-NX implementation

4.8.1 Configurate and programming

In this design there are two ways to program the FPGA, through the JTAG interface or through the external SPI flash with help of *Lattice Radiant Programmer,* a software tool aimed for the FPGA. The board is delivered with a pre-programmed SPI memory, please see the Quick Start Guide [RD1] and the User Guide for Nexus Platform [RD5] for more information about the prebuilt bitstream and how to programming the FPGA.

The CertusPro-NX supports multi-boot features so the users can easily switch between different FPGA bitstreams.

In Figure 4-18 the block scheme for the configuration is shown

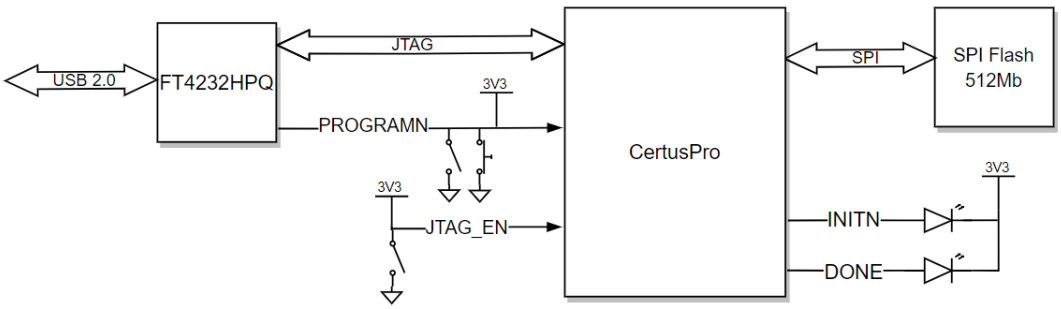

Figure 4-18 Programming the FPGA

There are three corresponding program signals.

1. PROGRAMN (input): Initiate configuration sequence when asserted LOW. This pulled up signal is connected to a switch (SW2) and jumper (JP3) for the user to set it to LOW activating configuration mode. The signal ca also be connected to pin BDBUS7 on the FTDI chip since there is one resistor that is not mounted.

2. INITN (Open Drain I/O pin): This signal is driven to LOW when configuration sequence is started, and the FPGA starts to load configuration data from the external SPI Flash.

3. DONE (Open Drain I/O pin): This signal indicate that the FPGA is in user mode. This signal is driven to LOW during configuration. It is released (high) to indicate completed configuration.

4.8.2 LED

On the board there are LEDs corresponds to the CertusPro-NX, see Table 4-6 for more information and Figure 4-19 for the board placement.

Table 4-6 LED correspond the CertusPro-NX

LED	Colour	Comment
D8	Red	Connected to INITN, indicates when errors occur during configuration
LED11	Green	Connected to DONE signal, indicates when configuration completed successfully
LED12	Green	Connected to GPIO
LED13	Green	Connected to GPIO
LED14	Green	Connected to GPIO
LED15	Green	Connected to GPIO

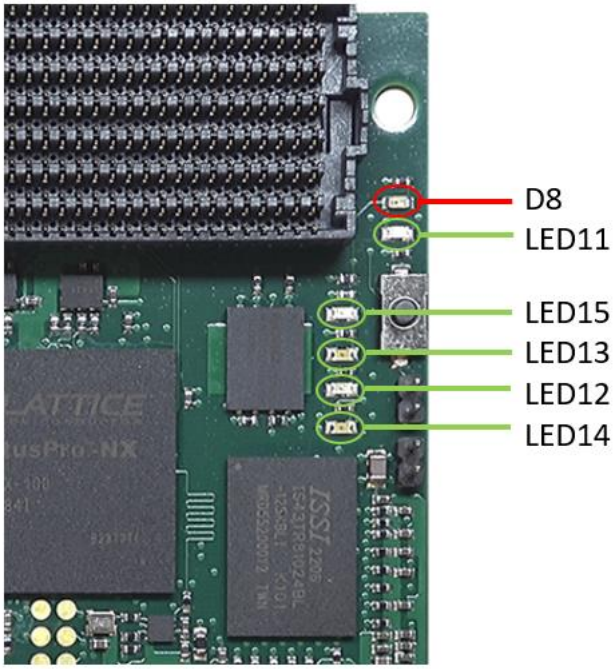

Figure 4-19 LED(11-15) and D8 board placement

4.8.3 JTAG

The JTAG link is routed via J2 (USB-C) through the FTDI chip. The FPGA has dedicated JTAG pins. To enable the JTAG interface the signal JTAG_EN must be HIGH. In this design this signal has a pull-up resistor and is therefore HIGH by default. The interface can be disabled by install the jumper (JP4), connected to GND.

4.8.4 SPI FLASH

The used Serial NOR Flash memory (MX25L51245GZ2I-08G) provides 512Mb of non-volatile storage. The device supports one, two or four I/O modes. The Flash memory is connected to the dedicated system configuration (sysCONFIG) pins on the FPGA and implemented as four I/O mode see Figure 4-20.

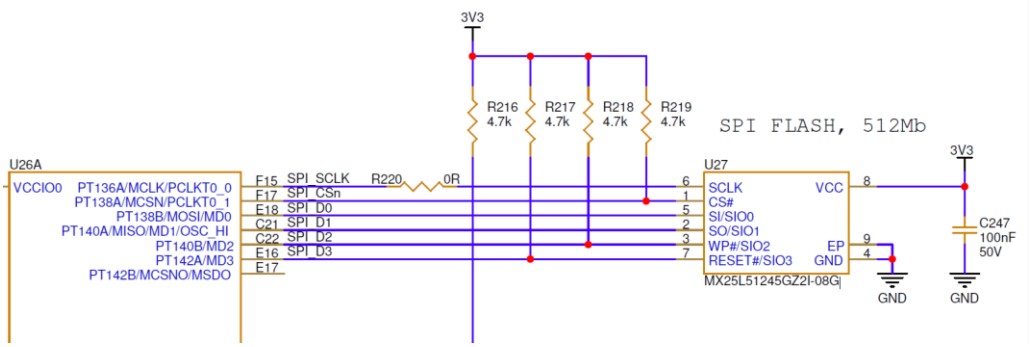

Figure 4-20 SPI Flash implementation

4.8.5 Oscillators and clocks input

Multiples clocks are providing inputs in order to have a flexible development environment. All clocks are to a dedicated clock input pin on different banks. Each clock input can be set to the reference clock to the global PLL. The PLL can divide the frequency by ÷2, ÷4, ÷8, ÷16, ÷32, ÷64, ÷128, and ÷1 (bypass). For more information about the clocking structure of the CertusPro-NX, please refer to [RD4].

Figure 4-21 shows the clock scheme for the FPGA.

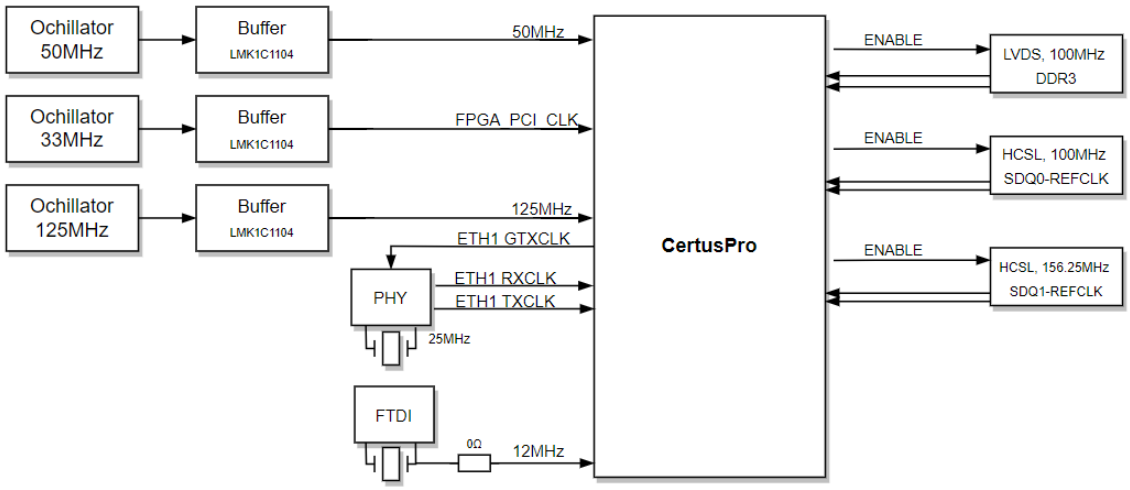

Figure 4-21 CertusPro-NX Clock Distribution scheme

The clock signals 50MHz, FPGA_PCI_CLK and 125MHz, are all buffered through LMK1C1104.

In MII mode the ETH1_GTXCLK is not used. The ETH1_RXCLK and ETH1_TXCLK are 25MHz and derived from the Ethernet PHY.

In GMII mode the ETH1_GTXCLK is used and set to 125MHz. The ETH1_RXCLK is running at 25MHz and derived from the Ethernet PHY.

The Ethernet PHY uses an external crystal of 25MHz.

The FTDI chip uses an external crystal of 12MHz, this clock signal is connected to the FPGA through a 0Ω resistor. By default, the resistor is not mounted and can be selected for future usage.

The clock oscillator that is aimed for the DDR3 interface is of LVDS type with a frequency of 100MHz and is connected to dedicated differential clock pair.

The two SerDes quads, Q0 and Q1 have one reference clock each (on the board) 100MHz and 156.25MHz, for more information about the SerDes quad see section *4.8.8*. The two-clock reference that are on the board are of HCSL type and is by default disabled.

4.8.6 DDR3 Memory

The design has a DDR3 memory interface connected to bank 3 supporting DQS logic. The bank is powered with 1V5.The used DDR3 memory (S43TR81024BL-125KBLI) provides 1GB volatile storage organized as 1G x 8 and have a JEDEC Speed grade DDR3-1600K. The implementation is shown in Figure 4-22. There are pins on the FPGA dedicated for the DDR3 operation and they are divided into DQS groups. One DQS group includes DQS, DQS#, eight DQ and one DM. A voltage reference pin is also needed for the implementation. For more information about the DDR3 interface please refer to [RD6].

In order to achieve correct termination and power supplies requirements, an external power management IC (TPS51206) is used.

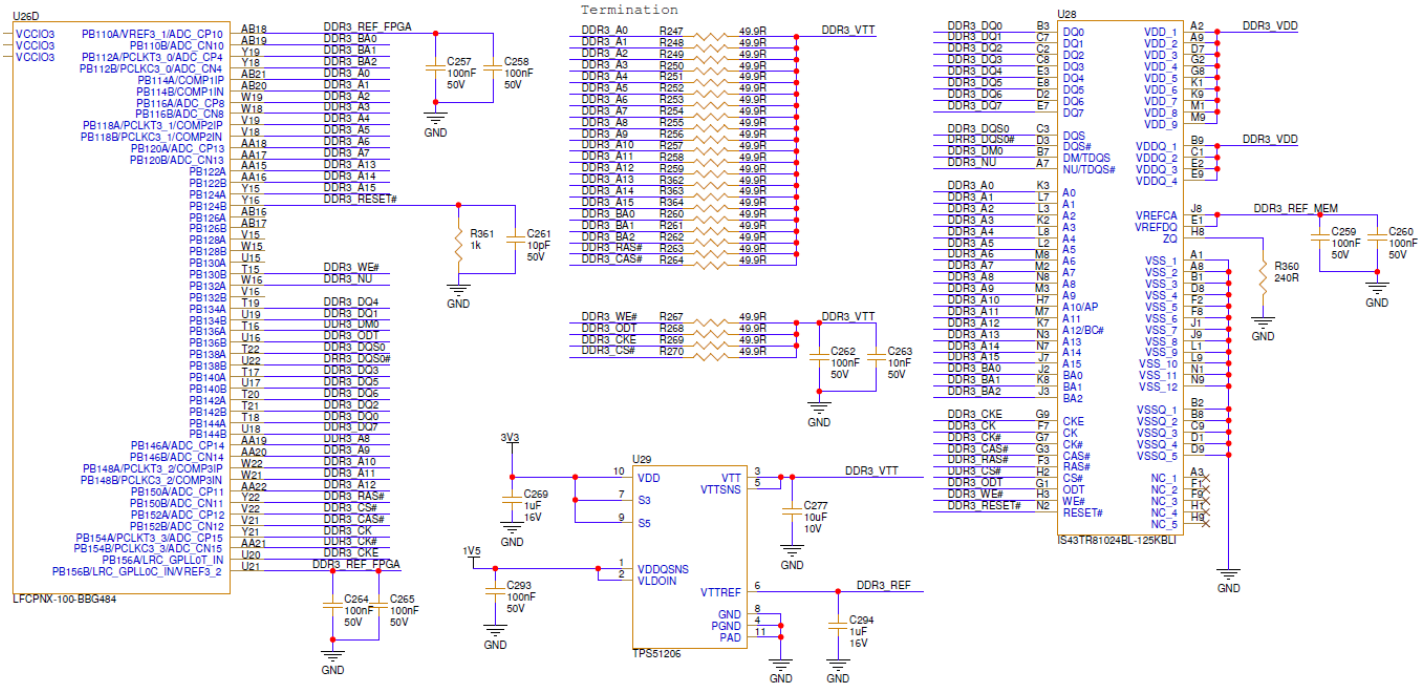

Figure 4-22 CertusPro-NX DDR3 memory implementation

4.8.7 Ethernet

The Ethernet interface is implemented on bank 6 using a 3V3 supply. Figure 4-23 shows the implementation for the interface. The RJ45 connector that is used has an integrated transformer. The Ethernet PHY transceiver that is used (KSZ9031) supports 10/100/1000Mbit/s Ethernet. PHY address is hard-wired to 2 (“010”). The transceiver uses an external 25MHz oscillator. Different clock configuration is used depending on which ethernet mode that is selected, se section *4.8.5* for more information.

The management signals for the PHY corresponding the GR740 is also connected to the bank, see Figure 4-26

The default IP address for the IP core that is provided in the pre-developed bitstreams is : 192.168.0.51

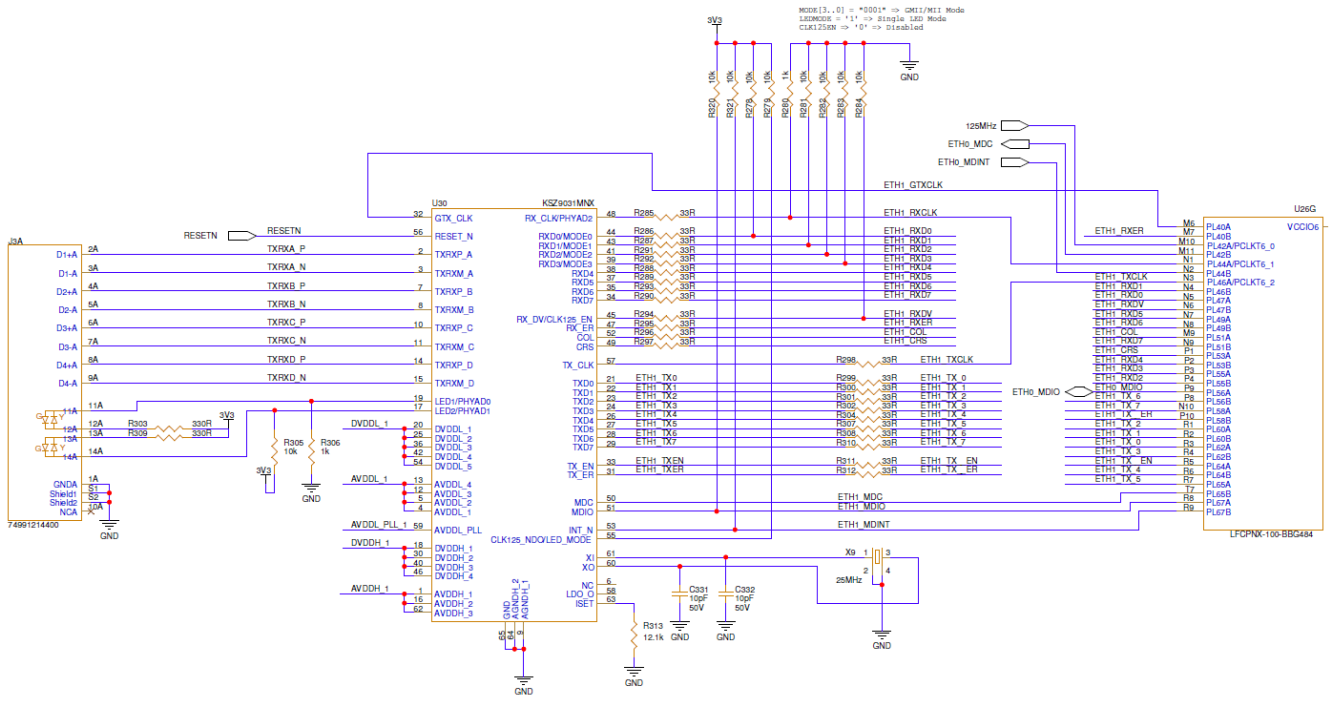

Figure 4-23 Ethernet implementation

4.8.8 SerDes

The CertusPro-NX provide two quads (Q0, Q1) with four SerDes channels and two reference clocks each. In this design both quads are used with two SerDes channels and both reference clocks, see Figure 4-24 for the SerDes implementation. All the SerDes channels and the external reference clocks are connected to the FMC+ connector, refer to section *4.10* for the signals and pinout. The reference clocks on the board are HCSL type of 156.25MHz for Q0 and 100MHz for Q1. R314 -R317 sets the termination impedance and it is set to 1.15kΩ which results in (RDIFF=) 100Ω. All corresponding differential signals for the SerDes are routed in the PCB layout with an impedance of 100Ω.

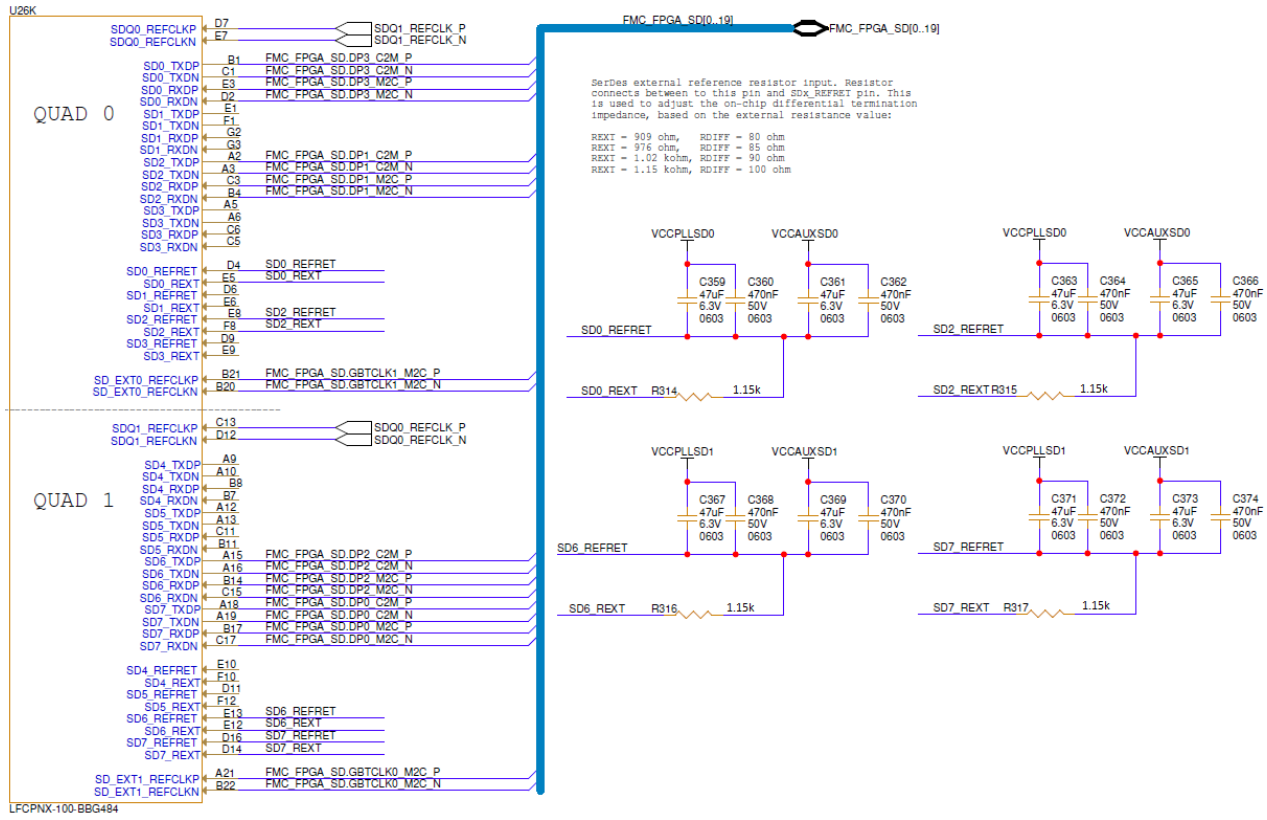

Figure 4-24 SerDes implementation

Frontgrade Gaisler AB
Kungsgatan 12 | SE-411 19 Goteborg | Sweden
+46 31 7758650 | frontgrade.com/gaisler

4.9 Intercommunication between GR740 and CertusPro-NX

4.9.1 PCI

Between the GR740 and CertusPro-NX the primary communication link is PCI, 32bit at 33MHz. The PCI-HOSTN signal to the processor have a pull-up resistor as default which results in that the FPGA will act as a target at the instantiation. There is also a pull-down resistor that is not mounted enabling an option to change the instantiation state. If one device is a target and the other master, then the REQ and GNT signals can be used as a point-to-point interface between the devices, otherwise, there is the need to use an arbiter for that purpose. The arbiter needs to be implemented in the FPGA design. In Figure 4-25 the block diagram for the PCI implementation is shown. In the schematics there are some NM/0R resistors [R236 – R241] to be able to change or modify the use of the arbiter. The PCI and the arbiter are implemented in bank 1 and 2 in the FPGA, which is supplied with 3V3.

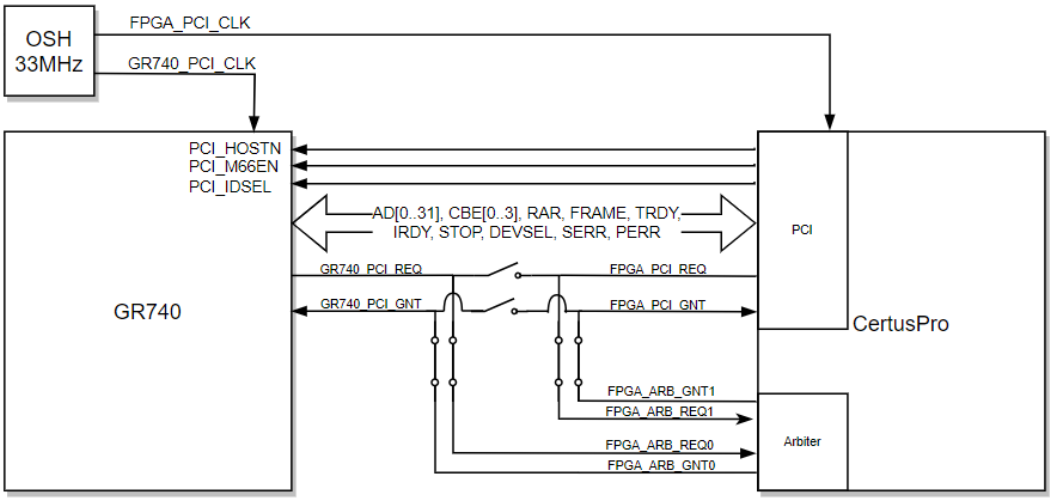

Figure 4-25 PCI interface

4.9.2 GMII/MII

Since the GR740 have shared pins for the PCI and Ethernet interface, an alternative is to use the GMII interface between devices. To use the GMII or MII interface user need to configure bootstrap signals for the GR740, refer to section *4.7.1.* Figure 4-26 shows the implementation for the GMII/MII intercommunication. The management signals (ETH0_MDC, ETH0_MDIO, ETH0_MDINT) from the GR740 is connected both to its own PHY and to the FPGA. This feature allows the GR740 to control both PHYs.

Note: If not used these management signals must be set to high-Z in the FPGA design.

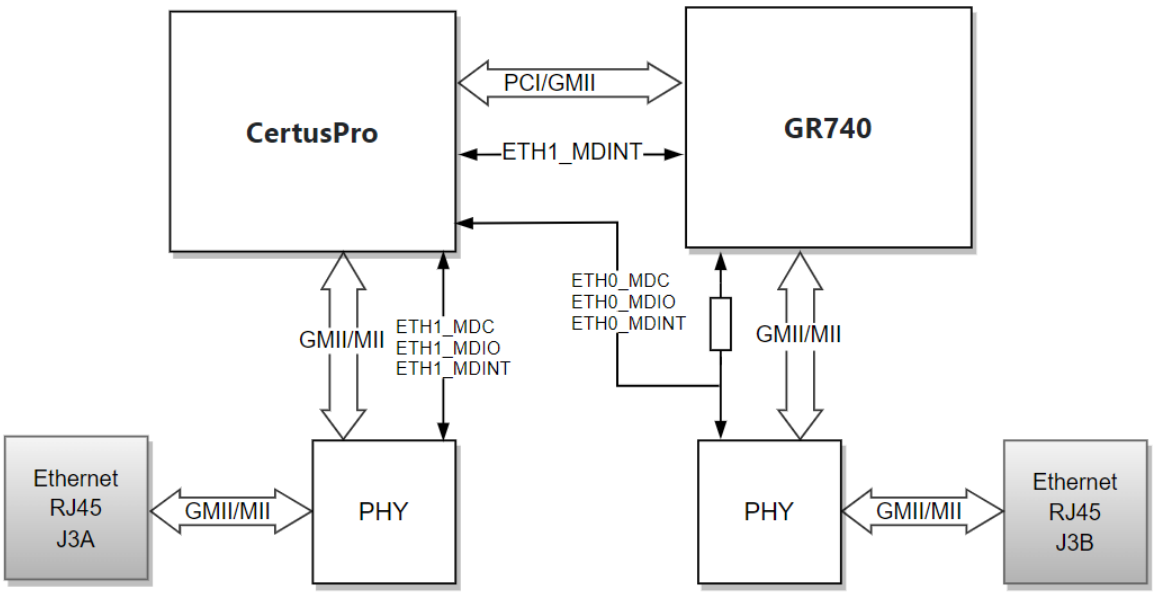

Figure 4-26 GMII/MII Intercommunication

In Table 4-7 the signals that are shared are listed.

Table 4-7 Shared pins on GR740 for PCI and Ethernet interface

Pin GR740	Signal Name	Signal Name	Pin CertusPro-NX
AB24	ETH1_TXD[7]	PCI_AD[31]	K19
AA23	ETH1_TXD[6]	PCI_AD[30]	J22
AB25	ETH1_TXD[5]	PCI_AD[29]	J19
AA22	ETH1_TXD[4]	PCI_AD[28]	K21
AC23	ETH1_TXD[3]	PCI_AD[27]	M13
AB23	ETH1_TXD[2]	PCI_AD[26]	J21
AC24	ETH1_TXD[1]	PCI_AD[25]	L15
AA21	ETH1_TXD[0]	PCI_AD[24]	L21
AD22	ETH1_TXEN	PCI_AD[23]	K13
AB21	ETH1_TXER	PCI_AD[22]	K22
AC17	ETH1_RXD[7]	PCI_AD[15]	M14

AE17	ETH1_RXD[6]	PCI_AD[14]	L22
AB17	ETH1_RXD[5]	PCI_AD[13]	N20
AD17	ETH1_RXD[4]	PCI_AD[12]	L19
AB16	ETH1_RXD[3]	PCI_AD[11]	N18
AE16	ETH1_RXD[2]	PCI_AD[10]	L20
AC16	ETH1_RXD[1]	PCI_AD[9]	M18
AD16	ETH1_RXD[0]	PCI_AD[8]	L18
AB15	ETH1_RXDV	PCI_AD[7]	N17
AE15	ETH1_RXER	PCI_AD[6]	M17
AA15	ETH1_COL	PCI_AD[5]	M16
AC15	ETH1_CRS	PCI_AD[4]	M15
AA14	ETH1_MDINT	PCI_AD[3]	N14
AC25	ETH1_GTXCLK	PCI_M66EN	M22
AB22	ETH1_TXCLK	PCI_HOSTN	L12
AA16	ETH1_RXCLK	PCI_IDSEL	M20

4.9.3 SpaceWire

There are four SpaceWire channels between the GR740 and the CertusPro-NX for intercommunication. GR740 uses SpaceWire port [4:7]. The SpaceWire signals are implemented as LVDS on bank 5 in the FPGA and is supplied with 1V8. The GR740 provides internal 100Ω termination on all LVDS inputs, and the CertusPro-NX provides a on chip programmable termination so there is no need for resistors in-between. All LVDS signals are routed in the PCB layout as point-to-point with an impedance of 100 Ω. See Figure 4-27 and Figure 4-28 for the pinout for the FPGA and GR740.

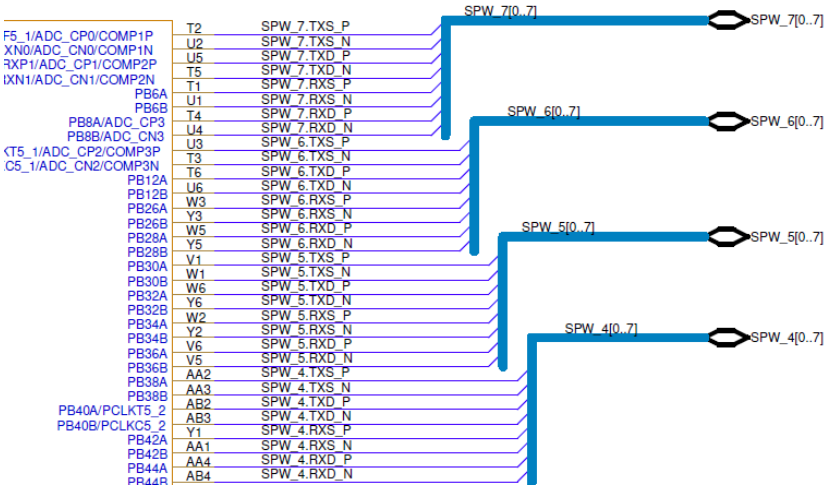

Figure 4-27 SpaceWire Implementation on the FPGA

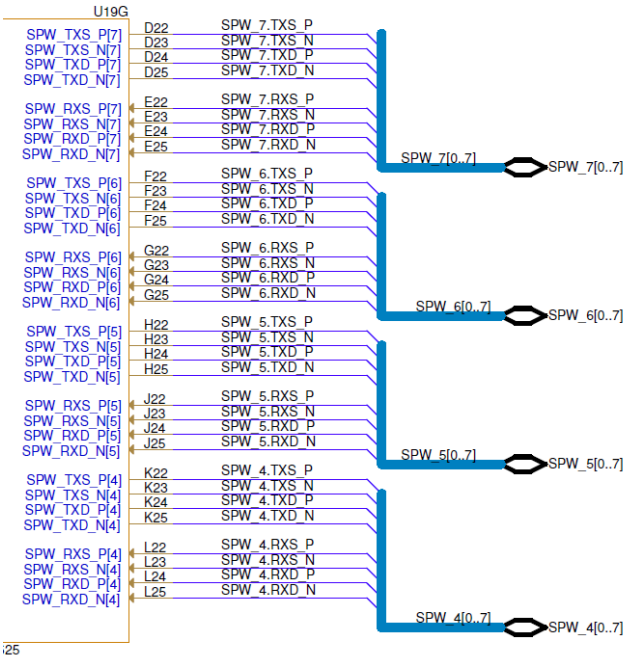

Figure 4-28 SpaceWire Implementation on the GR740

4.10 FMC+ connector

The *GR740-MINI* is equipped with an FMC+ connector (FPGA Mezzanine Card), that is connected to both the GR740 and CertusPro-NX, see Figure 4-29. The FMC+ connector is divided into two section, Low Pin Count (LPC) and High Pin Count (HPC) and is described for the two devices below:

1. CertusPro-NX: Bank 4 is connected to LVDS signals on the LPC part and have an adjustable voltage, default it is set to 1.8V (it must not exceed 1.8V).
   Bank 7 is supplied with 3V3 and is connected to the HPC section as single ended signals. CertusPro-NX contains two quads of four SerDes channels. In this design the first quad Q0, is connected to the SerDes channel (DP0) and a reference clock (GBTCLK0) in LPC and to the SerDes channel (DP2) in HPC. The second quad Q1 is connected to SerDes channels (DP1 & DP2) and reference clock (GBTCLK1) in the HPC

2. GR740: SpaceWire router interface port [0:3] are connected to the HPC part of the FMC+ connector.

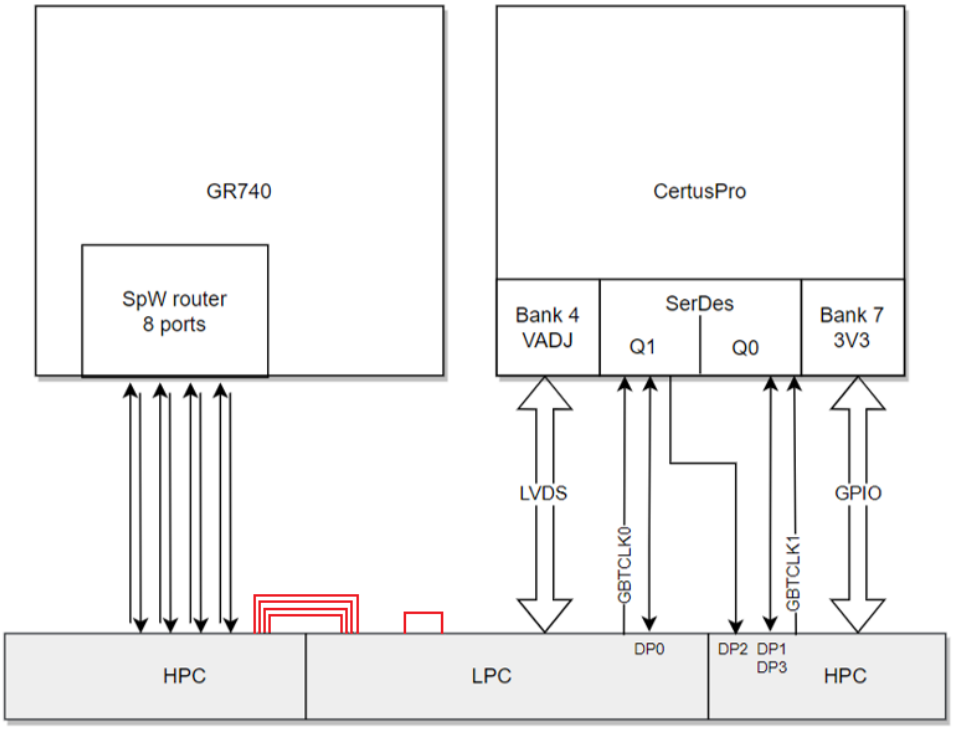

Figure 4-29 FMC+ connector scheme

NOTE: Some signals are connected to two different FMC connector pins, which is illustrated in Figure 4-29 in red, each line represents a differential pair. Due do this it is **IMPORTANT** to check the connection to the mezzanine card before connecting with the *GR740-MINI* board, see Appendix C and Table 4-8.

To avoid damage to the SPW interfaces due to common mode voltage the following actions should be performed before the equipment's that will be connected by SpaceWire are powered on.

● Before connecting any SpaceWire cables, make sure that there is no voltage difference between the different equipment grounds. E.g., measure the voltage between the different equipment grounds with a voltmeter. The result should be close to 0 V.

● After the SpaceWire cables are connected, make sure that the equipment grounds are low ohmic connected to each other. E.g., measure the resistance between the different equipment grounds with a multimeter in resistance mode. The result should be less than 1 Ω

This board is intendent to be used together with a mezzanine board. See the user's manual of the mezzanine board for information about the connection and grounding of the SpaceWire interface. Users using the board stand alone or design their own mezzanine board, must ensure that equipment's connected via SPW have grounds that are connected together.

Table 4-8 list all signals for the FMC+ connector is listed.

Note: In the column "comments" a notification is done whether the signal is connected to two different FMC connector pins (s.a *(FMC+) JX.NXX*) or other usage

Table 4-8 Pinout for FMC+ connector

Pin FMC	Signal Name	CertusPro-NX Bank	CertusPro-NX Pin	GR740 pin	Comment
LPC					
C2	DP0_C2M_P	Q1	A18		
C3	DP0_C2M_N	Q1	A19		
C6	DP0_M2C_P	Q1	B17		
C7	DP0_M2C_N	Q1	C17		
C10	LA06_P	4	W7		
C11	LA06_N	4	Y7		
C14	LA10_P	4	T8		
C15	LA10_N	4	U8		
C18	LA14_P	4	V7		
C19	LA14_N	4	U7		
C22	LA18_CC_P	4	AA7		
C23	LA18_CC_N	4	Y8		
C30	FMC_SCL	0	F18		
C31	FMC_SDA	0	G21		
C34	GA0				GND
C39	3PV3				
D1	FMC_PG_C2M	0	D22		
D4	GBTCLK0_M2C_P	Q1	A21		
D5	GBTCLK0_M2C_N	Q1	B22		
D8	LA01_CC_P	4	AB7		
D9	LA01_CC_N	4	AB8		

D14	LA09_P	4	W8		
D15	LA09_N	4	V8		
D17	LA13_P	4	AA8		
D18	LA13_N	4	AA9		
D20	LA17_CC_P	LA23_P			(FMC+) J4.D23
D21	LA17_CC_N	LA23_N			(FMC+) J4.D24
D23	LA23_P	4	U9		(FMC+) J4.D20
D24	LA23_N	4	T9		(FMC+) J4.D21
D26	LA26_P	4	AA14		(FMC+) J4.F25
D27	LA26_N	4	Y14		(FMC+) J4.F26
D32	3P3VAUX				
D35	GA1				GND
D36	3PV3				
D38	3PV3				
D40	3PV3				
G6	LA00_CC_P	4	AB9		
G7	LA00_CC_N	4	AB10		
G9	LA03_P	4	U10		
G10	LA03_N	4	T10		
G12	LA08_P	4	AA10		
G13	LA08_N	4	Y10		
G15	LA12_P	4	W10		
G16	LA12_N	4	V10		
G18	LA16_P	4	U11		(FMC+) J4.K37
G19	LA16_N	4	V11		(FMC+) J4.K38
G24	LA22_P	4	AB11		
G25	LA22_N	4	AB12		
G27	LA25_P	4	Y11		
G28	LA25_N	4	W11		
G39	VADJ				
H1	VREF_A_M2C	4	T14		
H2	PRSNT_M2C_L	0	E22		
H4	CLK0_M2C_P	4	U12		(FMC+) J4.K25
H5	CLK0_M2C_N	4	T12		(FMC+) J4.K26
H7	LA02_P	4	Y13		(FMC+) J4.K28
H8	LA02_N	4	W13		(FMC+) J4.K29
H10	LA04_P	4	V14		
H11	LA04_N	4	W14		
H13	LA07_P	4	AA11		
H14	LA07_N	4	AA12		
H16	LA11_P	4	AB13		
H17	LA11_N	4	AA13		
H19	LA15_P	4	AB14		
H20	LA15_N	4	AB15		
H25	LA21_P	4	V13		
H26	LA21_N	4	U13		
H40	VADJ				
HPC					
A2	DP1_M2C_P	Q0	C3		

A3	DP1_M2C_N	Q0	B4		
A6	DP2_M2C_P	Q1	B14		
A7	DP2_M2C_N	Q1	C15		
A10	DP3_M2C_P	Q0	E3		
A11	DP3_M2C_N	Q0	D2		
A22	DP1_C2M_P	Q0	A2		
A23	DP1_C2M_N	Q0	A3		
A26	DP2_C2M_P	Q1	A15		
A27	DP2_C2M_N	Q1	A16		
A30	DP3_C2M_P	Q0	B1		
A31	DP3_C2M_N	Q0	C1		
B1	CLK_DIR	0	E21		
B20	GBTCLK1_M2C_P	Q0	B21		
B21	GBTCLK1_M2C_N	Q0	B20		
F1	PG_M2C	0	F20		
F04	HA00_CC_P	7	L11		
F05	HA00_CC_N	7	L10		
F07	HA04_P	7	L5		
F08	HA04_N	7	L4		
F10	HA08_P	7	L3		
F11	HA08_N	7	L2		
F13	HA12_P	7	M2		
F14	HA12_N	7	M3		
F22	SPW_1.TXS_P			T22	
F23	SPW_1.TXS_N			T23	
F25	HB04_P	LA21_P	-		(FMC+) J4.D26
F26	HB04_N	LA21_N	-		(FMC+) J4.D27
F28	SPW_1.TXD_P			T24	
F29	SPW_1.TXD_N			T25	
F31	SPW_1.RXS_P			U22	
F32	SPW_1.RXS_N			U23	
F34	SPW_1.RXD_P			U24	
F35	SPW_1.RXD_N			U25	
F40	VADJ				
K07	HA02_P	7	G7		
K08	HA02_N	7	G6		
K10	HA06_P	7	G5		
K11	HA06_N	7	H6		
K13	HA10_P	7	K2		
K14	HA10_N	7	K1		
K25	HB00_CC_P	LA15_P			(FMC+) J4.H4
K26	HB00_CC_N	LA15_N			(FMC+) J4.H5
K28	HB06_CC_P	LA11_P			(FMC+) J4.H7
K29	HB06_CC_N	LA11_N			(FMC+) J4.H8
K31	SPW_2.RXS_P			R22	
K32	SPW_2.RXS_N			R23	
K34	SPW_2.RXD_P			R24	
K35	SPW_2.RXD_N			R25	
K37	HB17_CC_P	LA07_P			(FMC+) J4.H18

K38	HB17_CC_N	LA07_N			(FMC+) J4.H19
E2	HA01_CC_P	7	L9		
E3	HA01_CC_N	7	M8		
E6	HA05_P	7	K6		
E7	HA05_N	7	L6		
E9	HA09_P	7	L1		
E10	HA09_N	7	M1		
E12	HA13_P	7	M4		
E13	HA13_N	7	M5		
E21	SPW_0.TXS_P			V22	
E22	SPW_0.TXS_N			V23	
E24	SPW_0.TXD_P			V24	
E25	SPW_0.TXD_N			V25	
E27	SPW_0.RXS_P			W22	
E28	SPW_0.RXS_N			W23	
E30	SPW_0.RXD_P			W24	
E31	SPW_0.RXD_N			W25	
E33	SPW_2.TXS_P			P22	
E34	SPW_2.TXS_N			P23	
E36	SPW_2.TXD_P			P24	
E37	SPW_2.TXD_N			P25	
E39	VADJ				
J6	HA03_P	7	H8		
J7	HA03_N	7	H7		
J9	HA07_P	7	H5		
J10	HA07_N	7	H4		
J12	HA11_P	7	H1		
J13	HA11_N	7	J1		
J15	HA14_P	7	K10		
J16	HA14_N	7	K9		
J24	SPW_3.TXS_P			M22	
J25	SPW_3.TXS_N			M23	
J27	SPW_3.TXD_P			M24	
J28	SPW_3.TXD_N			M25	
J30	SPW_3.RXS_P			N22	
J31	SPW_3.RXS_N			N23	
J33	SPW_3.RXD_P			N24	
J34	SPW_3.RXD_N			N25	

REVISION INFORMATION

Issue	Date	Section / Page	Description
1.0	2023-10-23		First release of this document
1.1	2023-12-07	4.7.1	Updated Table 4-4, GPIO[11] set to LOW
		4.9.3	Added Figure 4-28 SpaceWire Implementation on the GR740
		4.10	Updated Table 4-8, changed CertusPro-NX Bank and CertusPro-NX Pin on signals DPx_x2x_x and GBTCLKx_M2C_x

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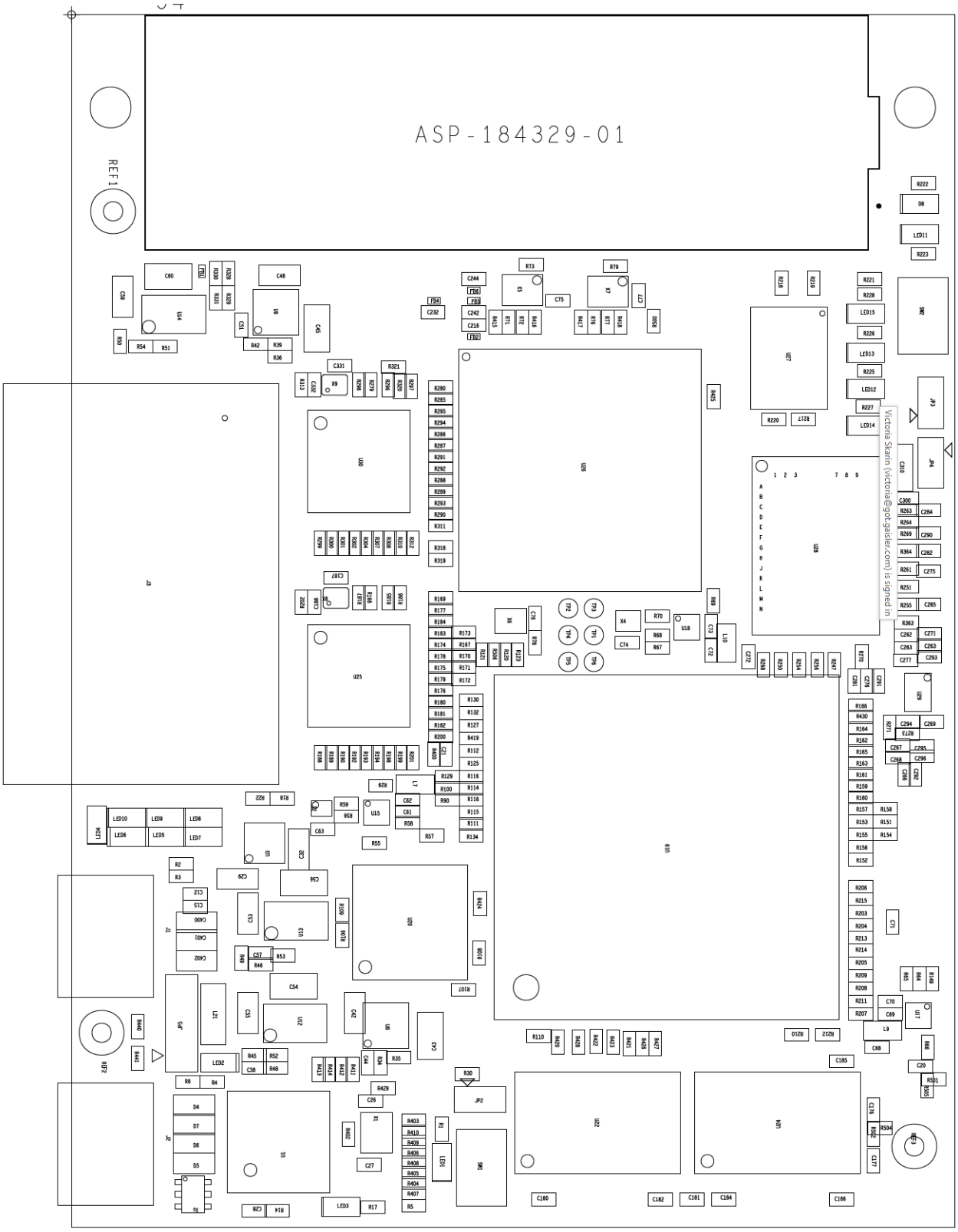
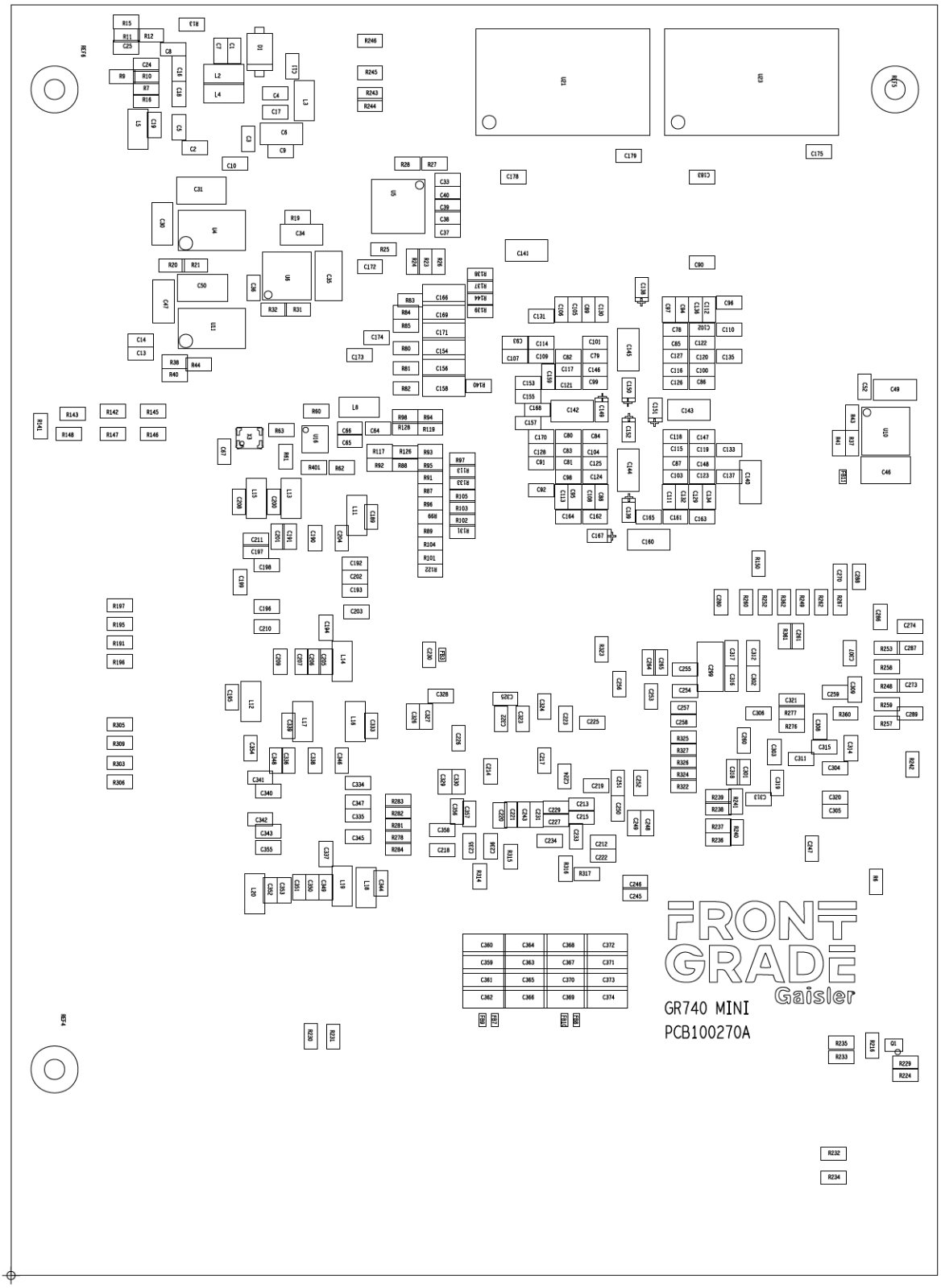
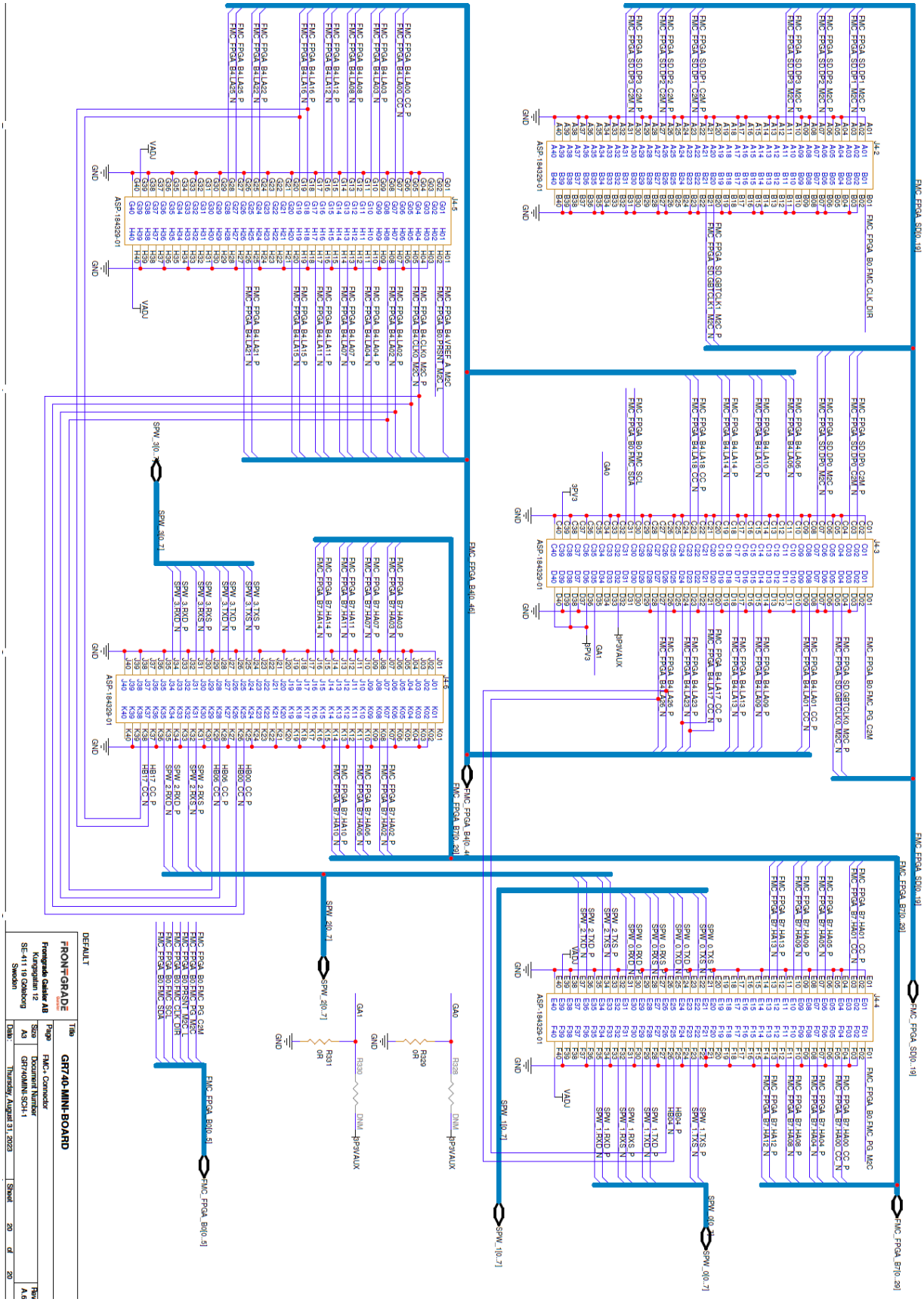
APPENDIX A



APPENDIX B



APPENDIX C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