Data Sheet & User Manual

GR-VPX-XCKU060 Carrier Board

GR-VPX-XCKU060

Features

- Xilinx XCKU060, in 1517 pin FCBGA package
- GR716B (initially with GR716A) microcontroller
- SODIMM DDR3 up to 8 GiB
- SPI flash for FPGA configuration (512 Mbit), for GR716 boot (256 Mbit), and for data (256 Mbit)
- Power, Reset, Clock and Auxiliary circuits
- Three FMC Mezzanine expansion connectors
- Scrubbing interface for FPGA
- Backplane I/F: SpaceWire (control), SpaceFibre (data), VPX utility management
- Frontplane I/F and drivers: 4x SpaceFibre, 2x SpaceWire, USB/FTDI UART/JTAG Links, USB I/F to FMC
- OpenVPX compatible, 6U format, Payload profile

Description

The GR-VPX-XCKU060 board features a Xilinx Kintex Ultrascale XCKU060 FPGA and a GR716 microcontroller acting as a supervisor for the FPGA. The board is equipped with three VITA 57.1 FMC connectors. It can be operated without any Mezzanine board but is specifically designed to be used with 1 to 3 GR-HPCB-FMC-M2 Mezzanine Boards connected, each with a Myriad™ 2 M2450 Processor. The GR-HPCB-FMC-M2 boards are not included with the GR-VPX-XCKU060 board.

Specifications

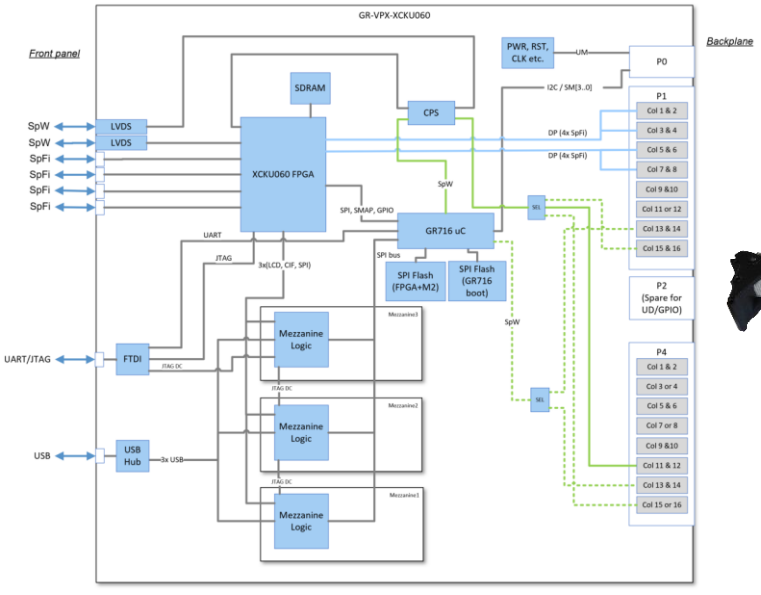
- System frequency GR716 uC: 20MHz, FPGA XCKU060: 50 MHz
- 5 x SpaceFibre links rated @ 3.125 Gbps and 2 x SpaceWire links @ 200 Mbps
- CIF and LCD data interfaces 16-bit running at 150 MHz. 24-bit interface tested allowing upper bound 1.44Gb/s full-duplex data transfer
- Typical power consumption <10W (excluding mezzanines)
- DC supply via OpenVPX backplane connector or via +5V/12V DC header for stand-alone use

Applications

The board is a commercial development board for prototyping of high-performance application such as:

- Earth Observation optical and radar payload processing
- Multi- and hyperspectral data compression
- Visual-Based Navigation acceleration
- Video processing
- AI/ML processing, such as:
  - Image segmentation (e.g. cloud screening and removal)
  - Object detection (e.g. fire detection)
  - Pose estimation

The applications can be allocated to the on-board FPGA or shared with technology implemented in up to three Mezzanine boards, configured either for increased performance or for redundancy applications. The control and supervision of the FPGA and Mezzanine boards is handled by a rad-hard microcontroller.



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1 INTRODUCTION

1.1 Scope of the Document

This document describes the design for the *GR-VPX-XCKU060* Development Board.

The main elements of this board are a Xilinx Kintex Ultrascale XCKU060 FPGA [RD1] and a GR716 microcontroller [RD2].

This board is designed and intended to be used with the GR-HPCB-MEZZ-M2 Mezzanine Board but is conceived also to fulfil the requirements of standard VITA57.1 for FMC Carrier boards [RD3].

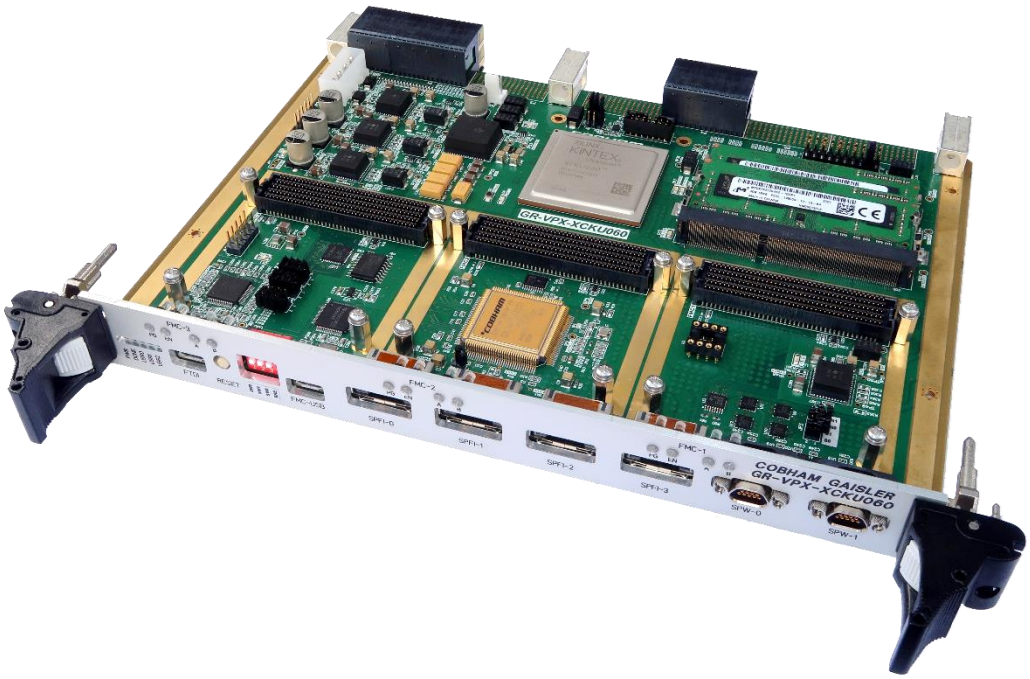

Figure 1 GR-VPX-XCKU060 Carrier Board

1.2 Reference Documents

[RD1] https://www.xilinx.com/products/silicon-devices/fpga/kintex-ultrascale.html

[RD2] https://www.gaisler.com/index.php/products/components/gr716

[RD3] ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard, https://vita.com/

[RD4] ANSI/VITA 65.0-2017 OpenVPX System Standard, https://vita.com/

[RD5] DRAFT VITA 78.00-2015 rev 1.15 SpaceVPX System Standard, https://vita.com/

[RD6] https://www.ti.com/tool/FUSION-DIGITAL-POWER-STUDIO

[RD7] https://www.xilinx.com/support/documentation/user_guides/ug576-ultrascale-gth-transceivers.pdf

[RD8] Datasheet and User Manual for GR-HPCB-FMC-M2 Mezzanine Board, doc. no GR-

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HPCB-FMC-M2-DSUM

[RD9] https://www.xilinx.com/support/documentation/user_guides/ug575-ultrascale-pkg-pinout.pdf

[RD10] GR-VPX-XCKU060 Board Package, see https://www.gaisler.com/index.php/products/boards/gr-vpx-xcku060

1.3 Document Revision Information

Version	Date	Section / Page	Description
1.0	2022-01-31		First approved issue.
1.1	2022-03-09	Page 1 Sec. 1.2	Editorial corrections of “Applications” and RD references.

1.4 Abbreviations

ASIC	Application Specific Integrated Circuit.
DCDC	DC DC Converter circuit
DDR	Double Data Rate
DSU	Debug Support Unit
ESA	European Space Agency
ESD	Electro-Static Discharge
ESTEC	European Space Research and Technology Centre
FP	Front Panel
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input / Output
I/F	Interface
I/O	Input/Output
LDO	Low-Drop-out
MUX	Multiplexer
PB	Push-Button
PCB	Printed Circuit Board
RTC	Real Time Clock
SOC	System On a Chip
SPFI	Space Fibre
SPW	SpaceWire

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2 ARCHITECTURE

This board is designed and intended to be used as an FPGA development board comprising the following main elements:

- Front panel connectors and interfaces
- Xilinx Kintex Ultrascale FPGA plus power supplies and associated components
- GR716 microcontroller plus associated components
- Three FMC Mezzanine board connectors for expansion
- On Board DDR3 Memory
- VPX Backplane interface and connectors

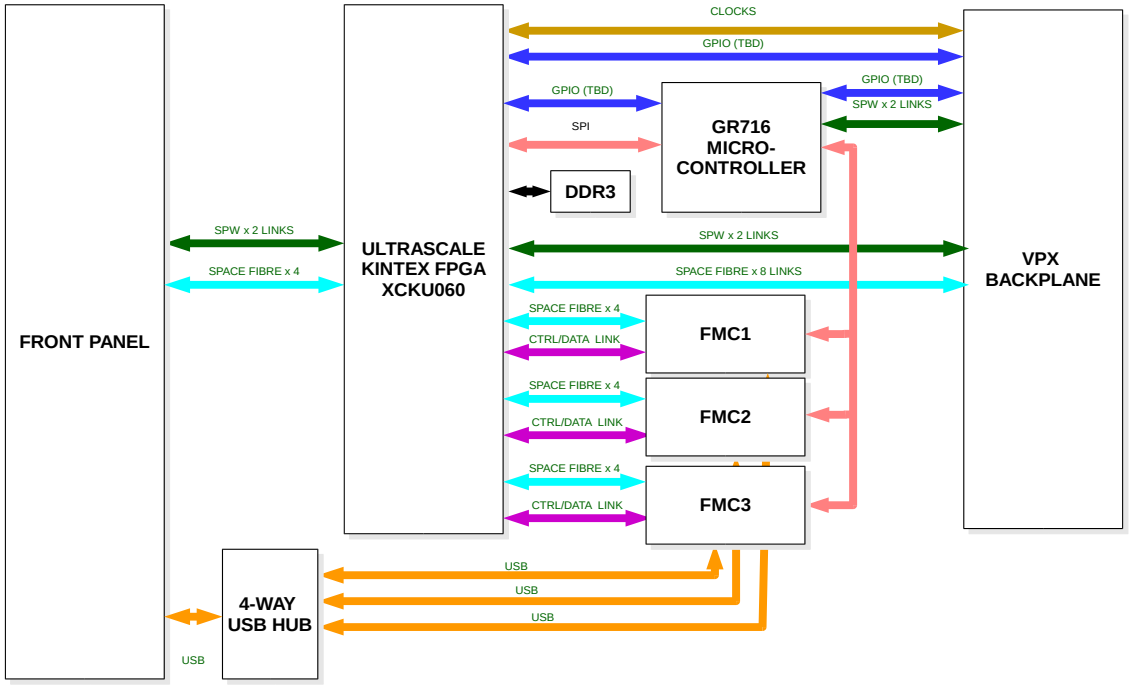

Figure 2 GR-VPX-XCKU060 Development Board

Three FMC Mezzanine board sites are implemented on the carrier board.

These interfaces have been initially designed to each accommodate a *GR-HPCB-FMC-M2* Mezzanine board with and MA2450 processing components, and the FMC interfaces are primarily assigned to accommodate this mezzanine board [RD8].

The pin definitions have been assigned to follow the assignment of the VITA57.1 specification [RD3] for FMC mezzanine boards to make the board suitable for use with other FMC-compatible mezzanine boards. The board can also be used without any Mezzanine boards.

It is designed to be used on a VITA 65 OpenVPX platform [RD4], specifically as a payload module compatible with the slot profile SLT6-PAY-4F1Q2T-10.2.1.

The main components and functional blocks described in section 3.

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The main interfaces of the board are described in section 5.

The mechanical format of the board is described in section 6.

3 CONFIGURATION AND INSTALLATION

3.1 Electrical installation

The board is designed for installation in a payload slot profile variant SLT6-PAY-4F1Q2T-10.2.1 as defined in the VITA 65 OpenVPX standard [RD4]. For operation, sufficient current capabilities of the +5V and +12V supply lines provided by the VPX backplane is to be confirmed, see below.

As an option, it can also be used in a stand-alone configuration, using the available headers for supply and communication, see section 5. Connection details for supply is described in sections 5.14 and 5.15.2. The connector allows for a dual supply with +5V and +12V DC. For the Carrier Board itself, only +5V is required, with a capability of at least 3A is recommended. The +12V is only routed to the FMC mezzanine connector. Capability required for the +5V and +12V leads depends on consumption of the Mezzanine boards.

3.2 Notes on VITA 57.1 compliance

With some exceptions the GR-VXP-XCKU060 board is designed to comply with the rules in the VITA 57.1 FMC standard [RD3]. Due to constraints on the Mezzanine board [RD8] it was designed for there are some deviations to the rules and recommendations listed below.

- VADJ is fixed to 1.8V and always enabled. Only mezzanines supporting 1.8V operation can be used.
  - Rule 5.123, and related rules 5.9, 5.10, 5.122)
- Two of the HPC pins (J9/J10, FMC signals HA07_P/N) are connected to a 3.3V bank (as I2C signals) while the other HAxy pins are connected to 1.8V banks. Hence an HPCB mezzanine for 1.8V VADJ with pins connected to HA may be subjected to overvoltage (3.3V).
  - Rule 5.1 (and to some extent related rules 5.3, 5.114)
- Rules about differential pairs are not fully implemented. For example, G6/G7 (LA00_P_CC/LA00_N_CC) do not connect to a differential pair on the FPGA. This makes it impossible to use LVDS signalling on those pins.
  - Recommendation 5.1
- The VREF mezzanine-to-carrier signals are not connected. This may degrade the performance of signalling standards that require a reference voltage (such as SSTL18 and HSTL18).
  - Rule 5.114 (and to some extent related rules 5.3, 5.4)
- Rules about clock capable pins are not fully implemented. Firstly LA00_CC_P/N, LA01_CC_P/N, LA17_CC_P/N, and LA18_CC_P/N are not connected to FPGA clock input capable pins. Secondly, although CLK0_M2C_P and CLK1_M2C_P connect to clock capable FPGA pins, the complementary CLK0_M2C_N and CLK1_M2C_N are disconnected. Hence LVDS clocks cannot be used for these

pins.

- For some pins: rules 5.24, recommendations 5.1, 5.5

- USB 2.0 signals are connected to LA33_P/N. These pins will be driven with 3.3V despite VADJ being 1.8V.
  - Rule 5.123, and related rules 5.9, 5.10, 5.122)

Some of the deviations above are allowed, if information is provided to the user as above, for example by the permissions below:

- Permission 5.10: If the signalling standard on Bank A does not require a reference voltage, then the mezzanine module may leave VREF_A_M2C unconnected
- Permission 5.13: VADJ may be used for other purposes beyond its use for Bank A IO supply voltage.

4 FUNCTIONAL BLOCKS

4.1 Memory

Several types of memory are required for the various functions:

Table 1 Summary of on-board memory

SPI Flash for FPGA configuration	512Mbit	Cypress (Spansion) S25FL512S
DDR3 for FPGA working memory	Up to 8 GB	SODIMM 204 connector, 64bit interface
SPI Flash for GR716 boot/data PROM	256Mbit	S25FL256L
SPI Flash for GR716 data PROM	256Mbit	S25FL256L

4.2 Xilinx Kintex Ultrascale FPGA

The board design incorporates a Xilinx XCKU060 FPGA in a FFVA1517C package.

This device has a footprint of 40 x 40mm.

The FPGA is a complex device requiring many high current and well-regulated power supplies.

The assignment signals and the VCC_IO must take account of assignment and compatibility rules, and allow a logical ‘flow’ of signals according to the geometrical placement of the components on the board.

The I/O Bank assignment is represented in Figure 3 below.

Notes:

- In Kintex Ultrascale, HP banks must operate at a VCC_IO voltage of 1.8V or lower.
- The HR banks (Banks 64 & 65 on XCKU060-FFVA1517) may be operated at 2.5V or 3.3V.
- LVDS signals should operate with a bank voltage of 1.8V for best compatibility with the internal LVDS termination capabilities.
- The DDR3 interface must operate with an I/O voltage of 1.5V.

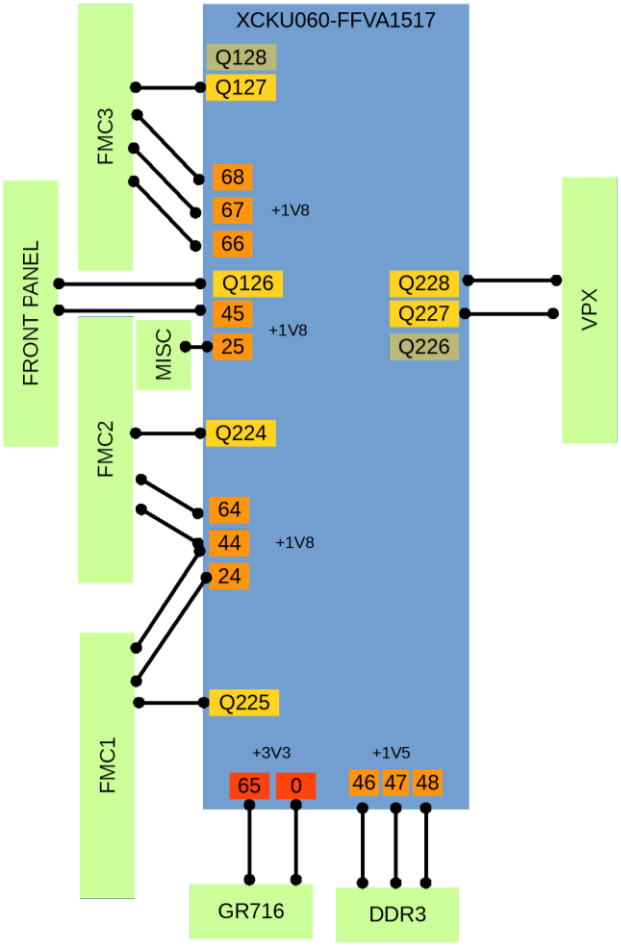

Figure 3 FPGA Bank Assignment

4.3 GR716 microcontroller

The GPIO pins are configured to allow the following interfaces of the *GR716* to be used:

- SPIM (for Boot program load from SPI memory)
- SPIM1 (for data load from SPI memory)
- DSU UART connection to FTDI USB circuit
- Application UART connection to FTDI USB circuit
- Redundant CMOS SPW1 pins connected to backplane via LVDS transceivers
- LVDS interface configured as SPW0
- I2C slave connection to SMBUS pins on VPX backplane
- I2C master connection for control/data connection to FMC circuits
- SPIO0 as master for control/data connection to FPGA
- SPIO1 as master for control/data connection to FMC circuits
- 22 x GPIO connected to FPGA for signalling purposes

4.4 Oscillators and Clock Inputs

The oscillator and clock scheme for the *GR-VPX-XCKU060 Board* is shown in Figure 4 below.

- The *GR716* can optionally use a 20MHz crystal to generate its system clock. However it is not fitted by default since current GR716
- Instead, the GR716 main system clock input is a 20MHz, 3.3V oscillator.
- For flexibility in clocking, a separate 50MHz 3.3V oscillator is used for the GR716 SPW_CLK input
- The FTDI UART circuit requires a dedicated 12MHz Crystal and generates its own internal oscillator with this crystal.
- The FPGA is supplied with two clocks for general use. CLK1 is a 50 MHz/1.8V oscillator soldered onto the board and CLK2 is a DIL 8 pin socket for a user defined 3.3 V oscillator.
- A 300 MHz LVDS oscillator is dedicated to the DDR3 interface.
- A 156.25MHz LVDS oscillator is provided for the GTH clock. This clock is connected to MGTREFCLK0, from which the other internal MGT clocks must be derived.
- Two LVDS backplane clocks (REF_CLK, AUX_CLK) are connected directly from backplane to the FPGA. The FPGA logic will have to determine how these clocks are used (nominally these are input clocks to the FPGA).

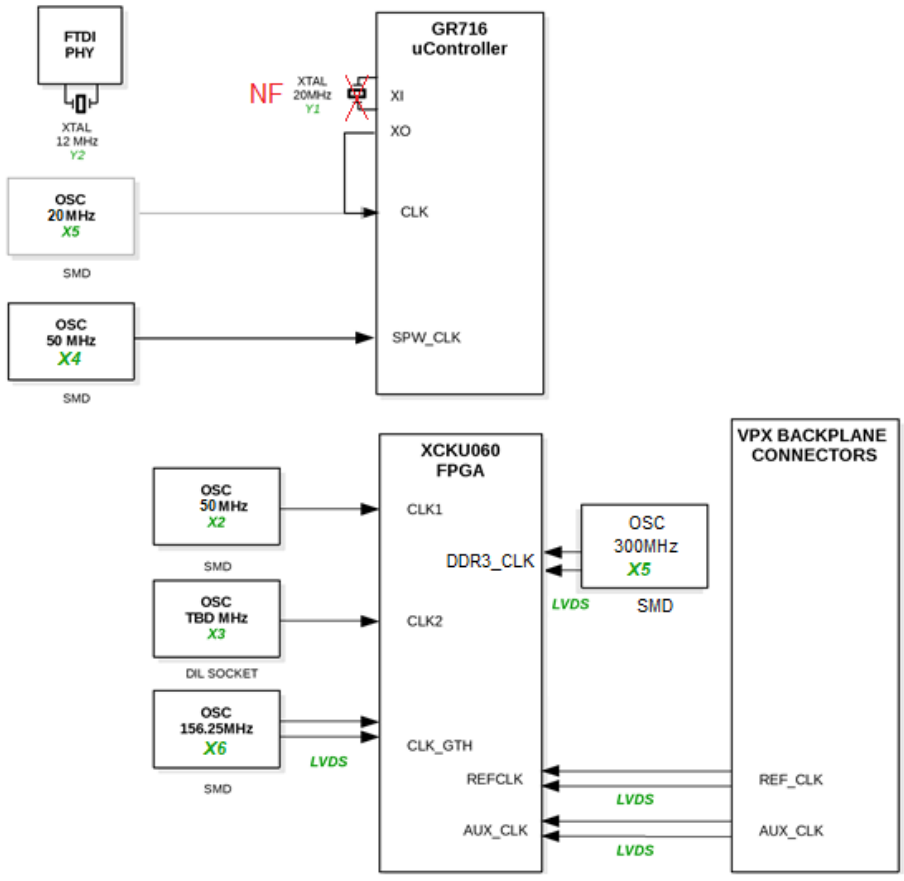

Figure 4 Board level Clock Distribution Scheme – GR-VPX-XCKU060

4.5 Reset Circuits

The reset scheme for the *GR-VPX-XCKU060* Board is shown in Figure 5 below.

The *GR716* has its own internal reset circuitry.

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A *TPS3705-33* reset supervisor provides a *RSTN* signal for the FPGA. The reset conditions for controlling the *RSTN* signal are:

- Front panel push button switch
- Backplane (VPX) System Reset
- +12V power good (PFO/PFI functionality of TPS3705-33)
- +3V3 power good (internal functionality of TPS3705-33)
- Watchdog (RESET_OUT_N for GR716)

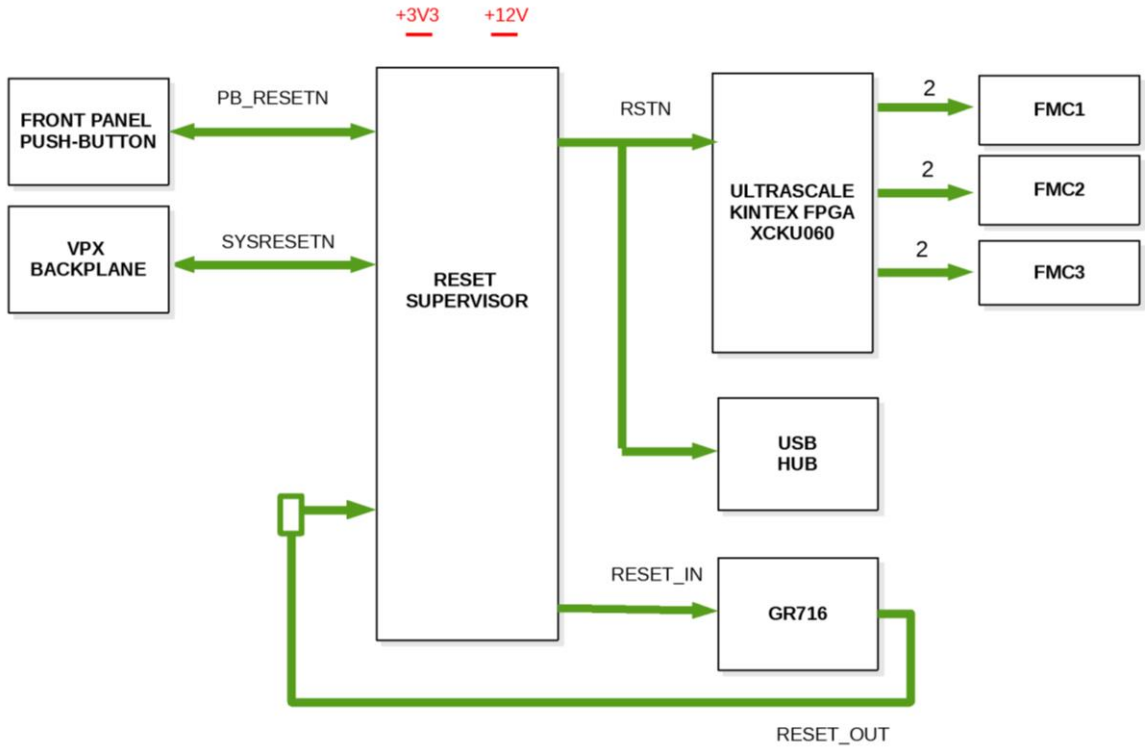

Figure 5 Board level Reset Scheme – GR-VPX-XCKU060

One I/O for each GR-HPCB-FMC_M2 mezzanine is a reset input controlled by the FPGA.

4.6 Power Supply and Voltage Regulation

4.6.1 Overview

The power supply system of the *GR-VPX-XCKU060* board requires many voltages to be generated and distributed, some of which have high current requirements (e.g. FPGA core voltage).

Typically, the power requirements must be over-dimensioned since the actual current consumption per rail is either unknown or varies depending on the application implemented in the FPGA logic.

The power circuitry occupies a significant PCB area (about one fifth), even with highly integrated commercial DC/DC modules are used.

A summary of the voltages required on the board is given in the table below.

Table 2 Summary of on-board voltages

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Device	Voltage	Dimensioning Current	Function
VIN	12V	-	From backplane to FMC slots
VIN	5V	-	From backplane to DCDC inputs
XCKU060	3.3V	2A	VCC_IO, SPI prom
XCKU060	1.8V	<0.5A	VCCAUX, VCC_IO
XCKU060	1.5V	>3A	For DDR3 interface
XCKU060	0.95V	>10A	Vcore
XCKU060	GTH_1.8V	<0.5A	MGTVCCAUX
XCKU060	GTH_1.2V	1A	MGTREF, MGTAVTT
XCKU060	GTH_1.0V	1A	MGTAVCC
DDR3	1.5V	>5A	
DDR3	0.75V	3A	DDR3 Termination voltage
GR716	3.3V	250mA	Assume single voltage mode using internal GR716 regulator for 1.8V
FMC-1	12V	1A	
FMC-2	12V	1A	
FMC-3	12V	1A	
Peripherals	3.3V	< 0.5A	Interface circuits
USB-HUB	1.1V	<0.3A	For USB Hub Vcore

4.6.2 Power sequencing

Power sequencing is required for the FPGA power rails. The only power domain that is active by default will be the PM_3V3 which provides the power for the *GR716* and the Power Monitor/Sequencer circuit.

Since some signals cross power domains, it will be necessary to carefully check the design for possible problems due to unintentional leakage across domains.

The power scheme to be implemented on the *GR-VPX-XCKU060* board is represented in Figure 6 below.

Power at a nominal input voltage of +12V is required from the VS1/VS2 and +5V from the VS3 input connections of the backplane. A 4-pin power connector is provided for connection to a bench top power supply when the board is used in a stand-alone configuration.

The 5V power supply provides power for the on-board DC/DC converters

The +12V power supply provides power to the 3 FMC slots.

A 3.3V power converter generates a dedicated 3.3V supply for the power sequencer.

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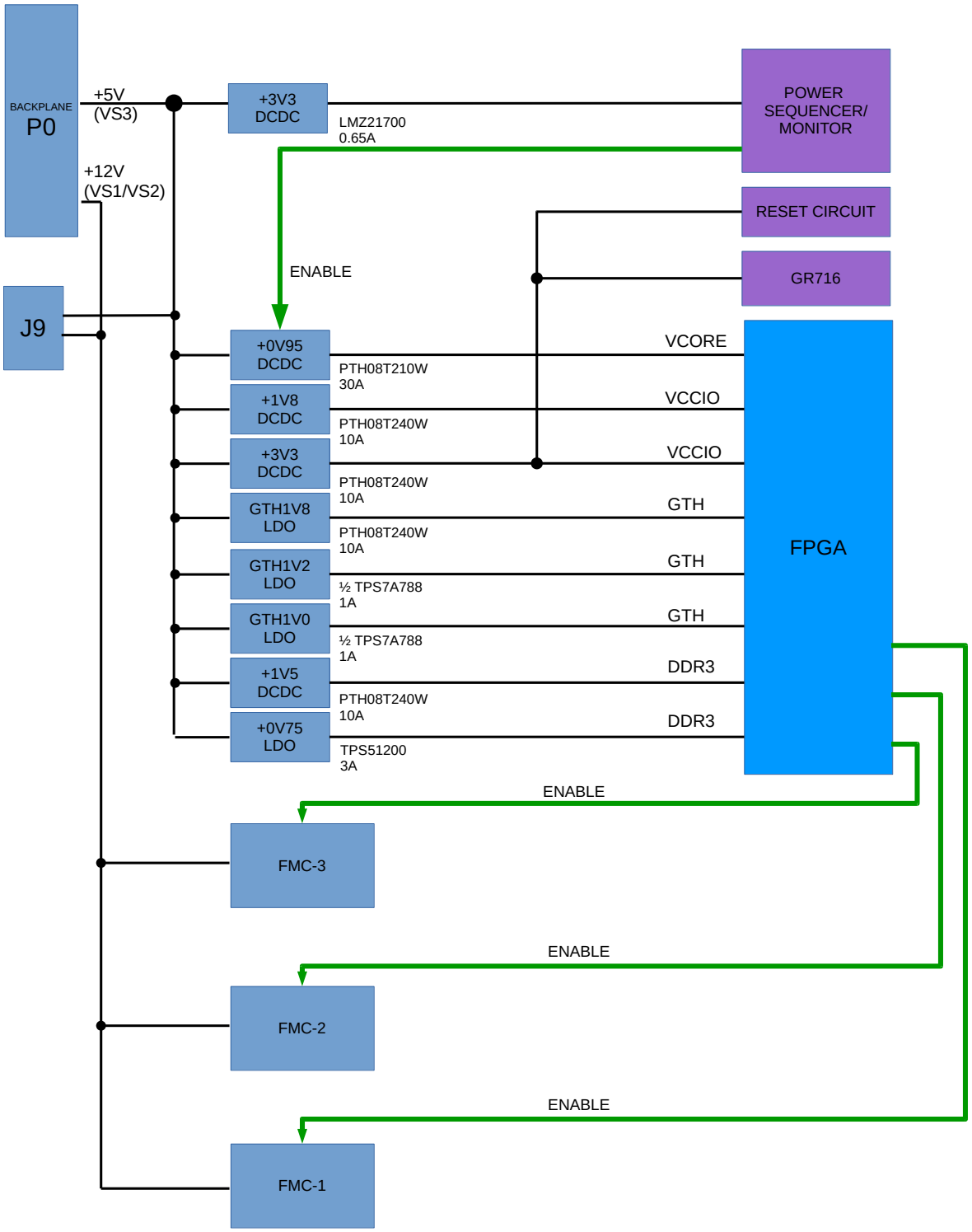

Figure 6 Power Regulation Scheme – GR-VPX-XCKU060

The power sequencer is a UCD9090 10-rail PMBus/I^{2}C addressable power supply sequencer and monitor which allows the monitoring of up to 10 voltage inputs and the programmed sequencing multiple outputs.

GPIO signals are used to control the enable signal of the +1V5 DC/DC converter and generate the power good signal PG_C2M.

Before delivery of the board, the UCD9090 is programmed with a default configuration file that specifies such things as rail sequencing order, sequencing delays, and over/under current/voltage fault limits. If the UCD9090 detects that a fault limit is reached on any of

the monitored rails, then it disables all on-board power converters. Depending on application, the need to change fault limits may arise. This can be done by reprogramming the device with the software *TI Fusion Digital Power Studio* [RD6] and a TI USB adapter (https://www.ti.com/lit/ml/sllu093/sllu093.pdf) connected to the J15 header on the GR-VPX-XCKU060. The software will read out the existing configuration and allows to change single parameters without generating a full programming file. A template programming file that includes rail names is provided in the BSP [RD10] for this board.

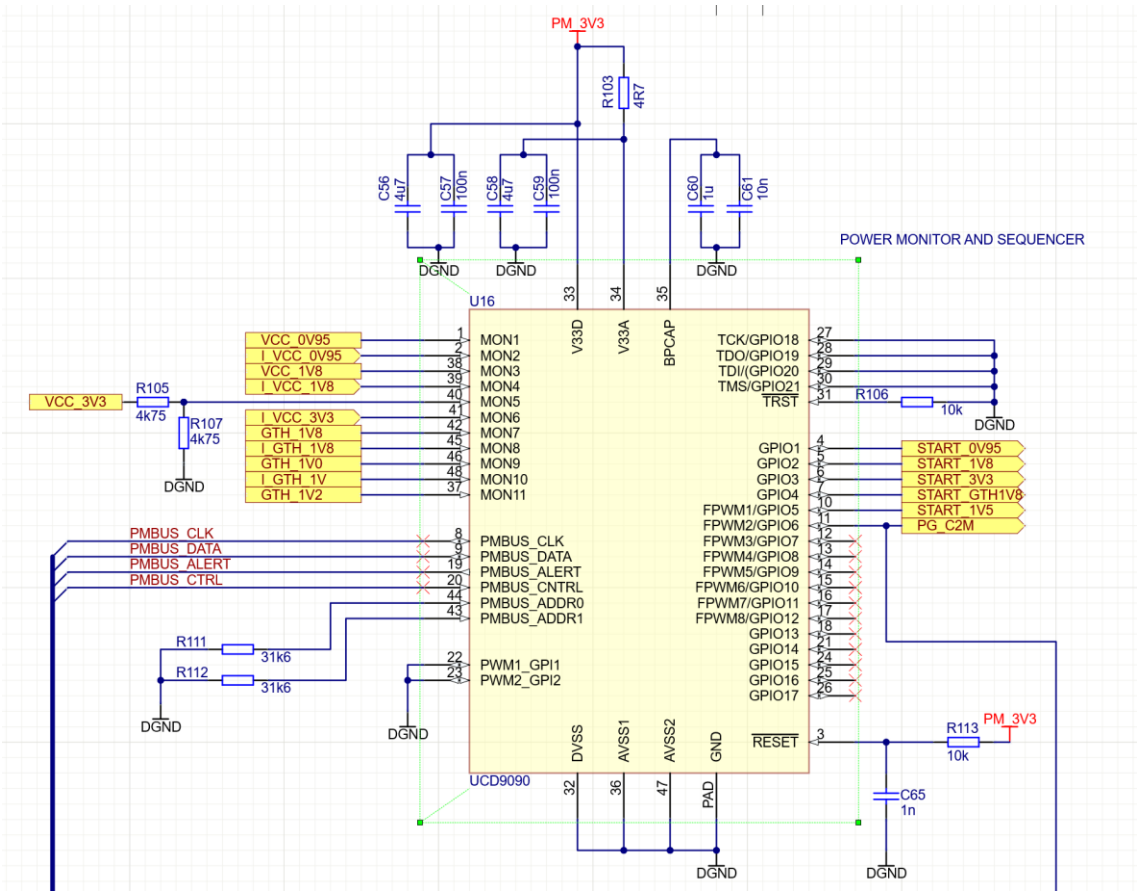

Figure 7 UCD9090 PMBUS Sequencer circuit

4.6.3 FMC Power Supplies

This board has three FMC slots, for interface expansion.

In a fully VITA57.1 compliant design, this would require each slot to have a programmable-controlled VADJ voltage supply, which can be set independently for each slot. This would require three additional independent DC/DC converters and I2C read-out and programming circuitry to fully accommodate these requirements.

However, for use with the envisaged *GR-HPCB-FMC-M2* mezzanines, this VADJ supply is not used, as the *GR-HPCB-FMC-M2* board requires only a 12V input supply and generates its' on-board voltages locally on the FMC mezzanine board. The local generation of supply voltages is necessary for the *GR-HPCB-FMC-M2* design to be able power up and shut down the circuits on the mezzanine board in a controlled manner.

In this *GR-VPX-XCKU060,* the VADJ power supply connection to all the three FMC slots

is fixed to have +1V8 I/O on all the FMC connections. This is compatible with the corresponding I/O bank voltage used for the FPGA connections to the FMC signals and is compatible with the intended use of the *GR-HPCB-FMC-M2* mezzanine boards. However, parts of the *GR-HPCB-FMC-M2* boards will be back powered through ESD diodes of I/O pins even when the on-board power generation is disabled.

Similarly, a fully compliant VITA57.1 compliant design would require VIO_M2C, VREF_A_M2C VREF_B_M2C signals connecting from each FMC connector to the FPGA I/O banks to allow full flexibility in the adaption of FMC boards to FPGA I/O standards.

However, this is not possible in this design as there are insufficient I/O banks available, and some I/O banks must be shared between the HA/HB sections of the FMC signals and between the FMC1, FMC2 and FMC3

These signals are therefore unconnected on the FMC interfaces.

See also an overview in section 3.2.

5 INTERFACES

5.1 Overview

Interfaces are present on the front panel, on the backplane and as board-only interfaces. Locations with PCB designators are indicated in Figure 8 and Figure 9 below.

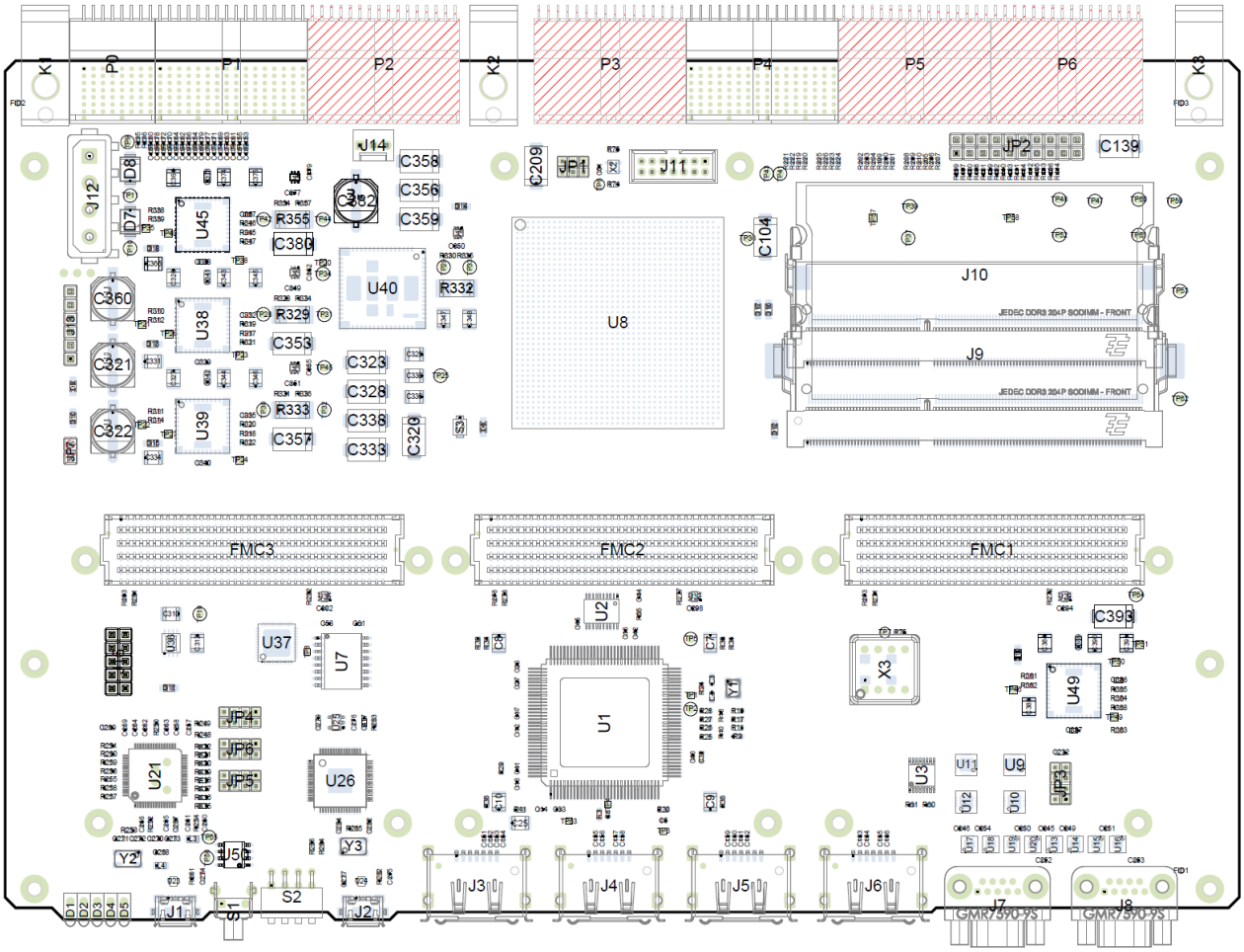

Figure 8 Top view

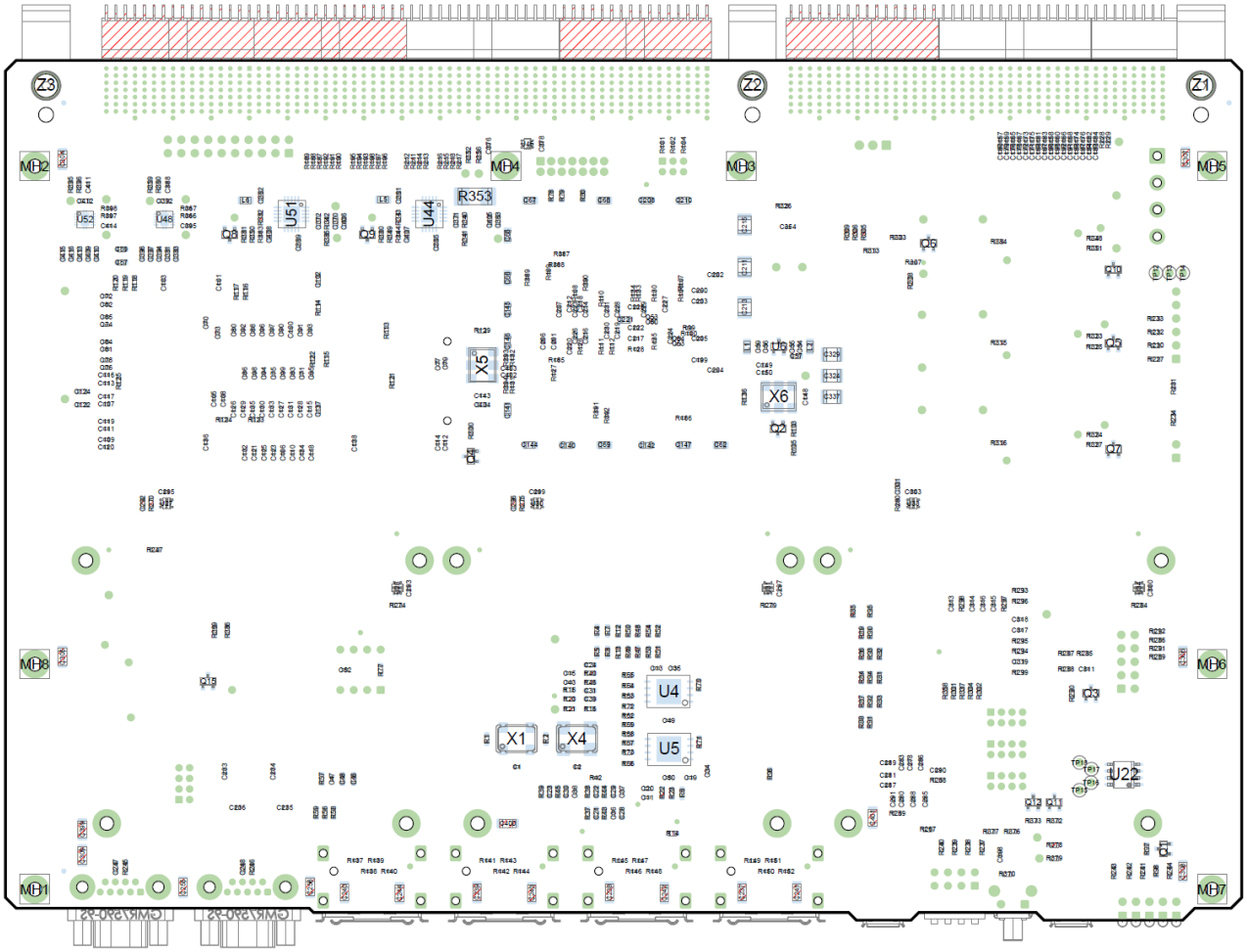

Figure 9 Bottom view

The three groups of interfaces are listed in subsections 0 to 5.4 below.

Detailed functionalities are described in subsections 5.5 to 5.17 below.

5.2 Front panel interfaces

The interfaces located on the front panel are illustrated and listed below.

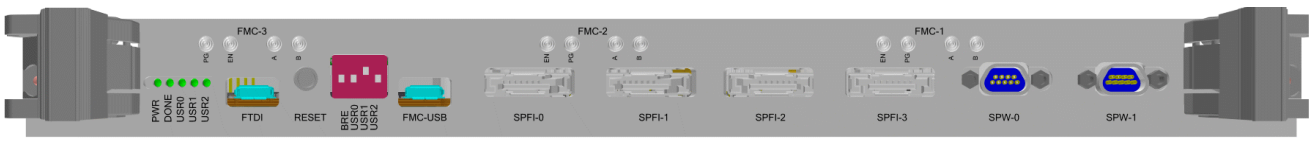

Figure 10 Front panel

Table 3 Front panel electrical interfaces

Interface	Marking	PCB id	Connected to	Protocol
SpaceFibre	SPFI-0	J3	FPGA, bank 224	SpaceFibre/CML
SpaceFibre	SPFI-1	J4	FPGA, bank 224	SpaceFibre/CML
SpaceFibre	SPFI-2	J5	FPGA, bank 224	SpaceFibre/CML
SpaceFibre	SPFI-3	J6	FPGA, bank 224	SpaceFibre/CML
SpaceWire	SPW-0	J7	Cross-point switch (external I/O selector: front panel or backplane)	SpaceWire, LVDS
SpaceWire	SPW-1	J8	FPGA, bank 68	SpaceWire, LVDS
USB	FMC-USB	J2	USB hub, for further transfer to USB ports	USB2.0

Interface	Marking	PCB id	Connected to	Protocol
			of Mezzanines 1, 2 and 3	
UART/JTAG	FTDI	J1	FTDI chip, for further transfer to JTAG0 (FPGA), JTAG1 (Mezzanines 1, 2 and 3 in daisy-chain) and UART (GR716)	USB2.0

Table 4 Front panel switches and buttons

Interface	Marking	PCB id	Connected to	Function
User DSU Break	BRE	S2	GR716 DSUBREAK signal	Sec. 5.16
User-controlled	USR0	S2	FPGA bank 65, pin AD14	Sec. 5.16
User-controlled	USR1	S2	FPGA bank 65, pin AF12	Sec. 5.16
User-controlled	USR2	S2	FPGA bank 65, pin AE12	Sec. 5.16
User reset	RESET	S1	Supervisor IC reset input, controlling reset of GR716 and FPGA	Sec. 5.16

Table 5 Front panel LEDs

Interface	Marking	PCB id	Connected to	Function
LED power on	PWR	D1	3V3 supply	3.3V on
LED FPGA done	DONE	D2	FPGA bank 0, pin AF11	FPGA initiation done
LED User 0	USR0	D3	FPGA bank 65, pin AF15	FPGA/User-controlled
LED User 1	USR1	D4	FPGA bank 65, pin AH12	FPGA/User-controlled
LED User 2	USR1	D5	FPGA bank 65, pin AG12	FPGA/User-controlled
Reserved for Mezzanine LED	FMC-1/2/3 EN	N/A	N/A	Controlled by Mezzanine, see e.g. [RD8]
	FMC-1/2/3 PG			
	FMC-1/2/3 A			
	FMC-1/2/3 B			

5.3 Backplane interfaces

The interfaces located on the backplane are listed below.

Table 6 Backplane electrical interfaces

Interface	PCB id	Connected to	Protocol
SpaceFibre DPN1	P1	See section 5.5	SpaceFibre/CML
SpaceFibre DPN2			
SpaceFibre DPN3			
SpaceFibre DPN4			
SpaceFibre DPR1			
SpaceFibre DPR2			
SpaceFibre DPR3			
SpaceFibre DPR4			
SpaceWire CPN	P4 (for 6U board)	See section 5.6	SpaceWire, LVDS
SpaceWire CPR			
Other signals	P0, P1, P4	See section 5.13	

5.4 On-board interfaces

The on-board interfaces are listed below, major internal as well as those available by headers.

Table 7 On-board electrical interfaces

Interface	PCB id	Connected to	Protocol
SPI (internal)	See section 5.7		
I2C (internal)	P0	See section 5.8	
GPIO (internal)	See section 4.3		
FTDI (USB/JTAG)	J11	See section 5.9 and Table 3	
Optional power header for stand-alone operation	J12	See section 5.14	
Optional SM-bus	J13	See section 5.15.3	
Optional FPGA fan	J14	See section 5.15.4	
Optional PM bus	J15	See section 5.15.5	

Table 8 On-board switches and buttons

Interface	PCB id	Connected to	Function
SelectMAP	JP1	See section 5.16.2	
FPGA spare	JP2	See section 5.16.3	
SpW cross-point switch settings	JP3	See section 5.16.4	
UART and JTAG access	JP4, JP5, JP6	See section 5.16.5	

Table 9 On-board LEDs

Interface	PCB id	Connected to	Function
FPGA initiation	D6	The LED is turned off during FPGA INIT phase and turned on when INIT is complete.	
+12V in	D9	+12V input is good to use, see section 5.14.	
+5V in	D10	+5V input is good to use, see section 5.14.	
+3.3V rail is above a threshold	D11	The LED is turned on when 5 V power is provided and the on-board generated PM_3V3 rail is above a threshold. Note that PM_3V3 supplies power sequencer (see Figure 7).	
All on-board generated secondary supplies are above a threshold	D12	This LED is controlled by the UCD9090 power sequencer and the behaviour is programmable. See section 4.6.2.	
Power Good 1V8	D13	The specifies supplies have reached nominal levels and are good for use.	
Power Good 0V95	D14		
Power Good 3V3	D15		
Power Good GTH_1V2	D16		
Power Good GTH_1V8	D17		
Power Good GVH_1V0	D18		
Power Good 1V5	D19		

5.5 SpFi

SpaceFibre interfaces are provided between the elements listed in the table below.

The “FPGA SerDes pins” column indicates which GTH channel is used (XnYm) and which bank. For example “224-1” means bank 224 channel 1 which is composed of the four pins MGTHTXP1_224, MGTHTXN1_224, MGTHRXP1_224 and MGTHRXN1_224. The meaning of the “Destination” varies. For “Front Panel” link it indicates the label under the corresponding eSATA connector. For backplane links (DPN/DPR), the VPX connector and column are indicated. Since a SpaceFibre lane fits in an ultra-thin pipe (one column) only the column number is indicated. For FMC the Vita 57.1 lane name is indicated. For example, DP2 is composed of FMC pins A26, A27, A6 and A7 (signal names DP2_C2M_P, DP2_C2M_N, DP2_M2C_P and DP2_M2C_N).

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Table 10 List of SpaceFibre interfaces

Tab	FPGA SerDes pins	Destination	Function
1	X1Y3, 224-3	Front Panel, SPFI-0	Data Interface
2	X1Y2, 224-2	Front Panel, SPFI-1	Data Interface
3	X1Y1, 224-1	Front Panel, SPFI-2	Data Interface
4	X1Y0, 224-0	Front Panel, SPFI-3	Data Interface
5	X1Y19, 227-3	DPR_SPFI_1, P1 col 1	Redundant Data Interface
6	X1Y18, 227-2	DPR_SPFI_2, P1 col 2	Redundant Data Interface
7	X1Y17, 227-1	DPR_SPFI_3, P1 col 3	Redundant Data Interface
8	X1Y16, 227-0	DPR_SPFI_4, P1 col 4	Redundant Data Interface
9	X1Y15, 228-3	DPN_SPFI_1, P1 col 5	Nominal Data Interface
10	X1Y14, 228-2	DPN_SPFI_2, P1 col 6	Nominal Data Interface
11	X1Y13, 228-1	DPN_SPFI_3, P1 col 7	Nominal Data Interface
12	X1Y12, 228-0	DPN_SPFI_4, P1 col 8	Nominal Data Interface
13	X0Y12, 127-0	FMC1-LPC0, DP0	Expansion Option
14	X0Y11, 127-1	FMC1-HPC1, DP1	Expansion Option
15	X0Y10, 127-2	FMC1-HPC2, DP2	Expansion Option
16	X0Y9, 127-3	FMC1-HPC3, DP3	Expansion Option
17	X0Y8, 126-0	FMC2-LPC0, DP0	Expansion Option
18	X0Y9, 126-1	FMC2-HPC1, DP1	Expansion Option
19	X0Y10, 126-2	FMC2-HPC2, DP2	Expansion Option
20	X0Y11, 126-3	FMC2-HPC3, DP3	Expansion Option
21	X1Y4, 225-0	FMC3-LPC0, DP0	Expansion Option
22	X1Y5, 225-1	FMC3-HPC1, DP1	Expansion Option
23	X1Y6, 225-2	FMC3-HPC2, DP2	Expansion Option
24	X1Y7, 225-3	FMC3-HPC3, DP3	Expansion Option

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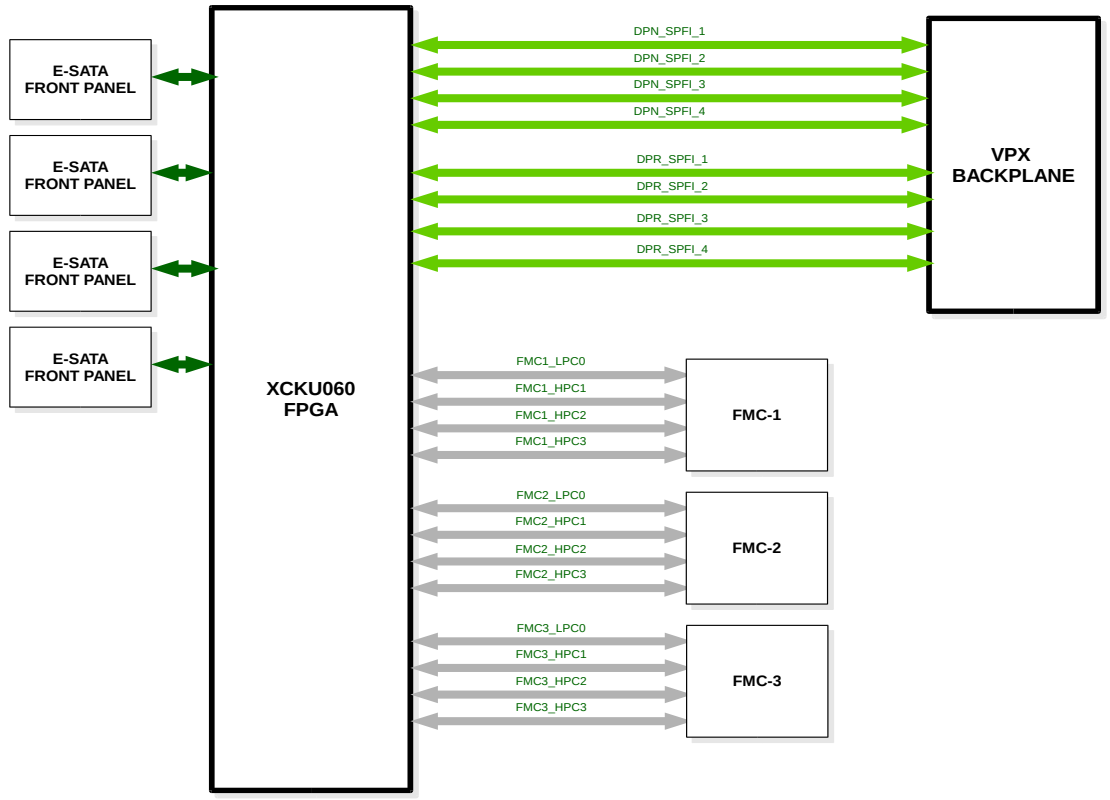

Figure 11 SpaceFibre Connections

The SPFI interfaces are be implemented using the built-in GTH Transceiver circuits of the Xilinx XCKU060 FPGA.

Each interface is composed of 2 differential signals (one TX and one RX), routed as very high-speed differential pairs.

As required by the SpaceFibre physical layer, each signal line is AC coupled using 150 nF capacitors and is connected to DGND with 100 kΩ bleed resistors.

Dedicated low noise power supplies (1.0 V, 1.8 V and 1.2 V) are implemented for the GTH transceivers ([RD7]).

The main clock input for the transceivers is a 156.25 MHz LVDS oscillator (see section 4.4). This allows the PLL to generate standard SpaceFibre line rates of 5.0, 2.5 and 1.25 Gb/s (multiplication by 64 to 10 GHz and divided by 2, 4, or 8) as well as 6.25 and 3.125 Gb/s (multiplication by 80 to 12.5 GHz and division by 2 or 4). It is connected as MGTREFCLK0 of bank 226. This is the centre bank of the RS power supply group (see Figure 1-6 in [RD9]) and can therefore supply a clock for all these banks (see section “Reference Clock Selection and Distribution” in [RD7]). As shown in Table 10 this includes all front-panel and backplane links as well as FMC3 expansion link. Only the FMC1 and FMC2 expansion links cannot be clocked from this source.

Additionally, each FMC link includes a mezzanine to carrier clock signal connected to MGTREFCLK0 of the corresponding GTH banks.

5.6 SpW Interfaces

The board implements up to three simultaneous SpaceWire Links distributed between the VPX backplane, GR716 microcontroller, Ultrascale FPGA, and External Front panel connectors.

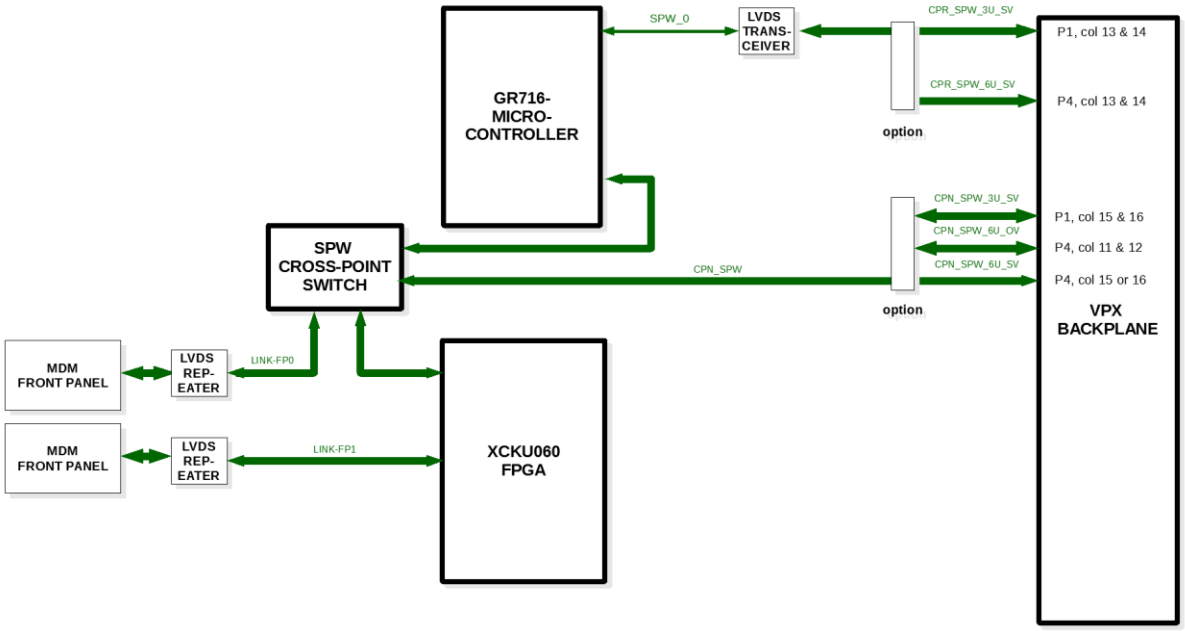

Figure 12 On-Board SpaceWire Connections

SpaceWire interfaces are identified between the following elements:

Table 12 List of SpaceWire interfaces

	Source	Destination	Function
1	FPGA	Front Panel 1	Data Interface
2	FPGA	Cross-point Switch	Data Interface
3	GR716	Cross-point Switch	P1 Control Plane Interface (prime)
4	GR716	VPX (CPR_SPW_3U_SV) VPX (CPR_SPW_6U_SV)	P1 Control Plane Interface (red.) P4 Control Plane Interface (red.)
5	Cross-point Switch	Front Panel 0	Data Interface
6	Cross-point Switch	VPX (CPN_SPW_3U_SV) VPX (CPN_SPW_6U_OV) VPX (CPN_SPW_6U_SV)	P1 Control Plane Interface (prime) P4 Control Plane Interface for 6U backplane P4 Control Plane Interface for 6U backplane

Each interface requires 4 LVDS pairs (8 pins).

Although the FPGA and GR716 have built-in LVDS drivers and receivers LVDS repeaters are used for both front panel and backplane links for increased robustness.

The GR716 microcontroller has a second SpW interfaces that uses single-ended LVCMOS signals. It is connected to the backplane via a SN65LVDS050 LVDS trans-ceiver circuit.

A SpaceWire cross-point switch comprised of DS25CP512 devices is implemented to allow re-routing of some of the SpaceWire signals between FPGA/GR716/Front panel and Backplane as shown in Figure 12.

Default links are:

- SpW Control Plane from backplane is linked to the GR716.
- SpW links from the MDM connector on the front panel is routed to the FPGA

In debug or stand-alone (without backplane) use

- SpW Control Plane from backplane to the GR716 is emulated/replaced by the upper front-panel SpW port.

The mode of the Cross-Point Switch is set manually by means of jumpers depending on the test set up required.

For the backplane connections, a number of options for the destination pins have been defined, depending on whether the board will be installed in a 6U or 3U backplane system. These are implemented with zero-ohm resistors which must be defined at manufacturing time of the board.

The GR716 SpW signalling rate is controlled by software and an internal PLL. The max GR716 link rate is 100 Mbps. Max bitrate supported by the FPGA is 600 Mbps but will depend on instantiation.

5.7 SPI

SPI control interfaces are identified between the following elements:

Table 13 List of SPI interfaces

Master	Slave	Function
FPGA	FPGA configuration memory	Memory interface
FPGA	FMC1	Control Interface for FMC1
FPGA	FMC2	Control Interface for FMC2
FPGA	FMC3	Control Interface for FMC3
GR716 uC	Boot Memory	Memory interface
GR716 uC	Data Memory	Memory interface
GR716 uC	FPGA	Control interface
GR716 uC	Slave 0: FMC1 Slave 1: FMC2 Slave 2: FMC3	Shared SPI interface for FMC1/FMC2/FMC3 with separate Slave Selects

The FPGA requires an SPI configuration prom of 512 Mbit which contains the FPGA configuration data. This data is automatically loaded at power-up/reset over a dedicated SPI interface with the FPGA acting as the Master.

The remaining part of this subsection describes the specific case using the *GR-HPCB-FMC-M2* mezzanine boards connected to the FMC connectors and illustrates how SPI can be used. Each of the *GR-HPCB-FMC-M2* board has one Myriad™ 2 M2450 Processor.

The loading of the boot program for each of the Myriad devices is performed via an SPI interface with the FPGA as master. To allow parallel programming of the multiple modules, each has a separate SPI interface.

The *GR716 microcontroller* has a dedicated SPIM interface connected to a 256 Mbit SPI memory which is used to contain the boot program information for the microcontroller. This data is automatically loaded at power up with the *GR716* as master.

A second SPIM interface is connected to a second 256 Mbit SPI memory which is used to contain DATA information

The *GR716 microcontroller* has two additional SPI interfaces with the *GR716* acting as master. The first interface is connected to all the Myriad chips, sharing the MISO, MOSI

and CLK signals, but with one of four dedicated SPI Select signals.

A second SPI interface is connected between the *GR716* and *FPGA* for exchange of control and telemetry data. The *GR716* operates as the Master of this interface.

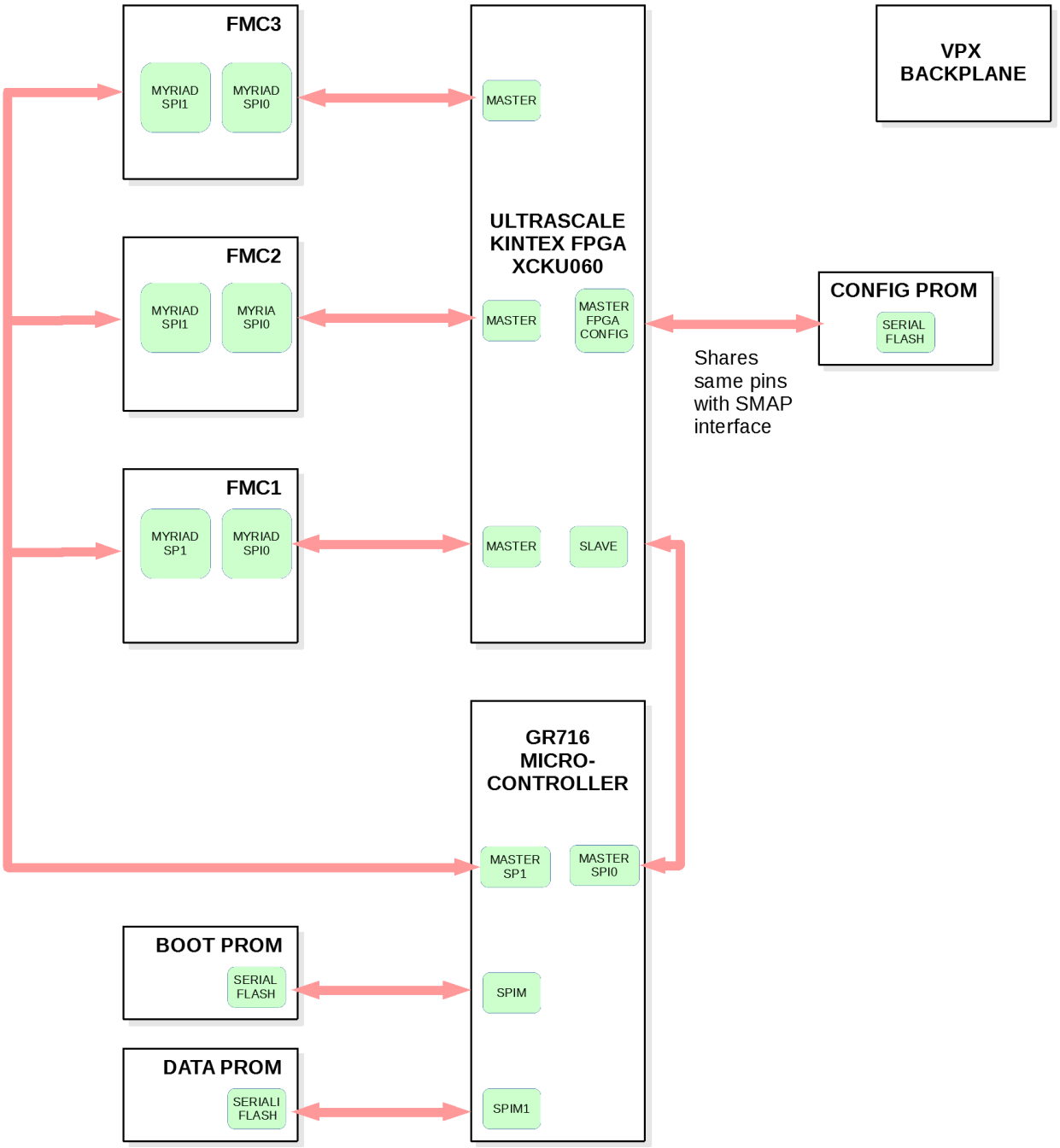

Figure 13 On-Board SPI Connections

5.8 I2C

I2C control interfaces are identified between the following elements:

Table 14 List of I2C interfaces

Master	Slave	Function
FPGA	FMC1	Control Interface for FMC1
FPGA	FMC2	Control Interface for FMC2
FPGA	FMC3	Control Interface for FMC3
GR716 uC	VPX Backplane	SMBus
GR716 uC	FPGA	Control interface
GR716 uC	Slave 0: FMC1 Slave 1: FMC2 Slave 2: FMC3	Shared I2C interface for FMC EEPROMs

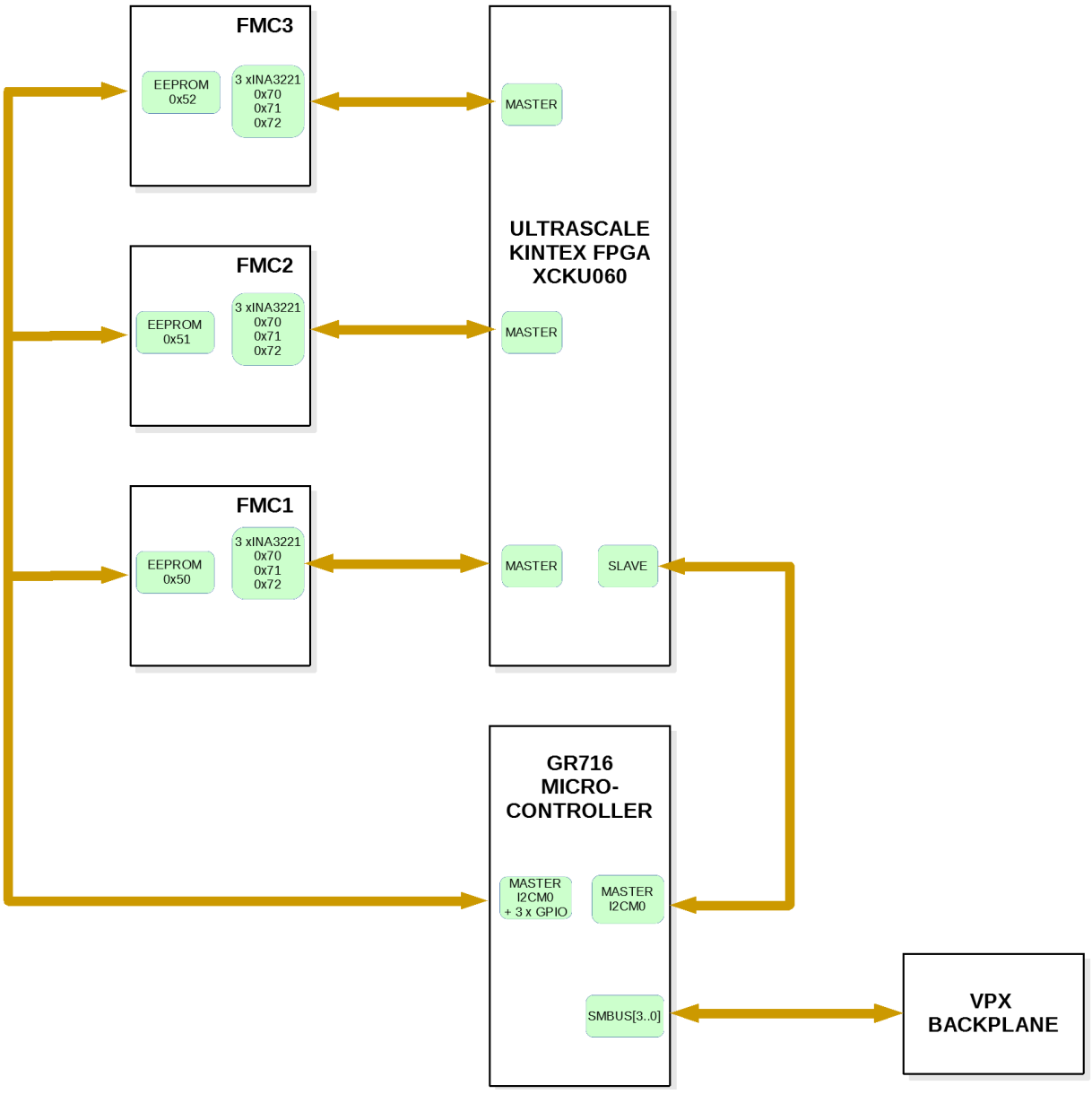

Figure 14 On-Board I2C Connections

5.9 FTDI (USB Serial/Jtag)

An FTDI FT4232 serial to USB interface chip is implemented on the board to allow an external PC to interface to the following serial interfaces

- *XCUK060 FPGA* JTAG interface
- *FMC* JTAG interface (daisy chain of 3 x FMC interfaces)
- *GR716 DSU* serial interface
- *GR716* UART-3 serial interface

The front panel interface connector is a standard USB Micro-AB style connector.

5.10 JTAG

The JTAG configuration on the board is shown in Figure 15.

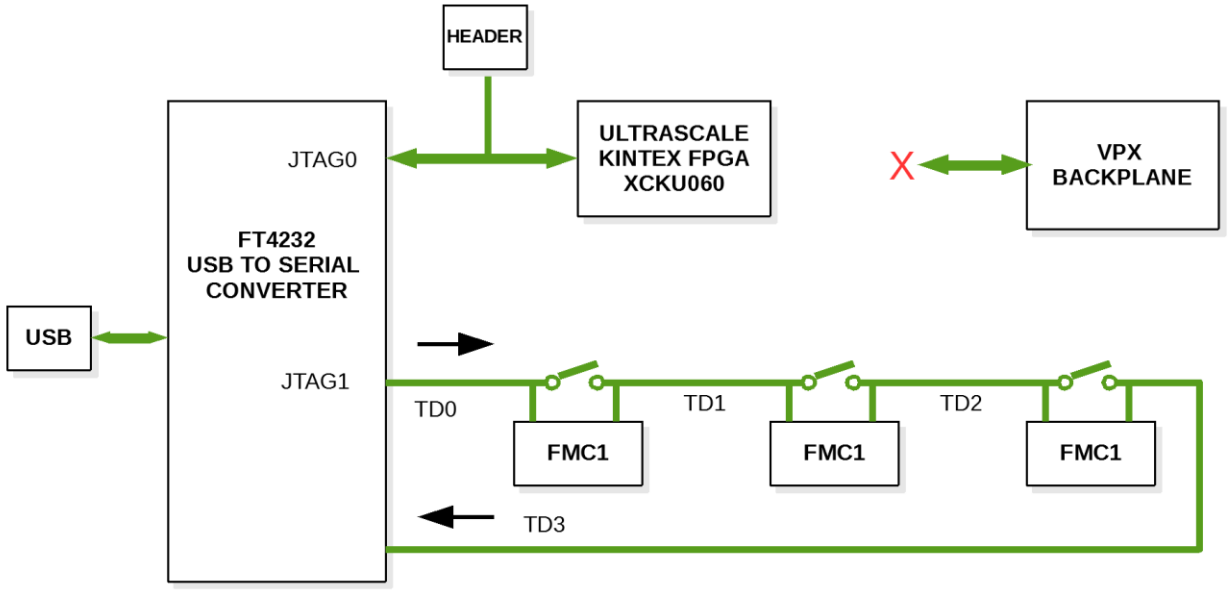

Figure 15 JTAG chain

The JTAG interface of the *FPGA* is connected to the FTDI-USB interface to allow an external JTAG DSU connection to the FPGA. This interface operates with 3.3V logic levels.

For debugging and direct JTAG programming using Xilinx tools, a dedicated connector header J11 is also available on the board.

A second JTAG chain is connected to the FTDI-USB interface to allow an external JTAG DSU connection to the devices on the FMC boards. The TDI-TDO signals of the 3 modules are daisy-chained using SPST switches. The state of the switches is controlled by the FMC signals 'Presence_Detect'. If an FMC board is present then the switch will be open, else the TDI-to-TDI connections will be short circuited by the switch. The VITA57.1 specification for the FMC board design requires that this interface operates with 3.3V logic levels.

The *GR716* does not have any JTAG functionality.

There are no connections to the VPX backplane JTAG pins.

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5.11 USB

The Myriad MA2450 chips on the *GR-HPCB-MEZZ-M2* board have a built in USB interface capable of supporting with a USB 2.0 and a USB3.0.

This interface can be used for booting and as a direct application interface for software running on the Myriad.

To have a single USB connector on the front panel for these interfaces, a 4 port USB hub device is required as shown in Figure 2.

The hub device is a Texas Instruments TUSB4041I Automotive 4-port high-speed 480-Mbps USB 2.0 hub. USB 3 is not supported.

Note that this USB interface is not related to the FTDI-USB interface described in section 5.9 and has a separate connector on the front panel.

5.12 FMC Interfaces

5.12.1 Overview

Three FMC Mezzanine board sites are implemented on the carrier board.

All three sites, FMC-1, FMC-2 and FMC-3 are LPC (low pin count interface) compatible. However, to make the interface compatible with the use of the *GR-HPCB-FMC-M2* board, some additional signals on the HPC section of the connector are required to be connected, and this interface is implemented as a 400 pin HPC type although it does not support the full HPC signal interface implementation of the VITA57.1 standard. Rules from VITA57.1 about clock capable signals (LA00, LA17 and LA22) are not followed. Neither are the rules about differential pairs. Hence most of the pins only support single-ended signalling standards.

In the subsections below the details of the FMC interface are described. The naming on signals and references to Mezzanine board features targets the *GR-HPCB-FMC-M2* board. The “Carrier Board” in the subsections below refers to this specific *GR-VPX-XCKU060* board. Statements including the “M2” device refers to the Myriad™ 2 M2450 Processor. For use with other mezzanine boards, this information

5.12.2 FMC Interface Summary

The main interfaces of the system are:

- FMC-Signal
  - LCD
  - CIF
  - SPI0
  - SPI1
  - USB
  - JTAG
  - Discrete Signals
    - SYS-RSTN
    - WAKEUP
    - HEARTBEAT[1..0]

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        - GA[1..0]
    - I2C (power measurement IC's)
- FMC-Power
    - +12V
    - Discrete Signals
        - ENABLE
        - PWR-GOOD
        - S[3..0]
- FMC-Auxiliary
    - I2C (FMC EEPROM)

The pinouts for the three connectors are illustrated in Figure 16, Figure 17 and Figure 18 below. Signals are described in sub-sections that follow.

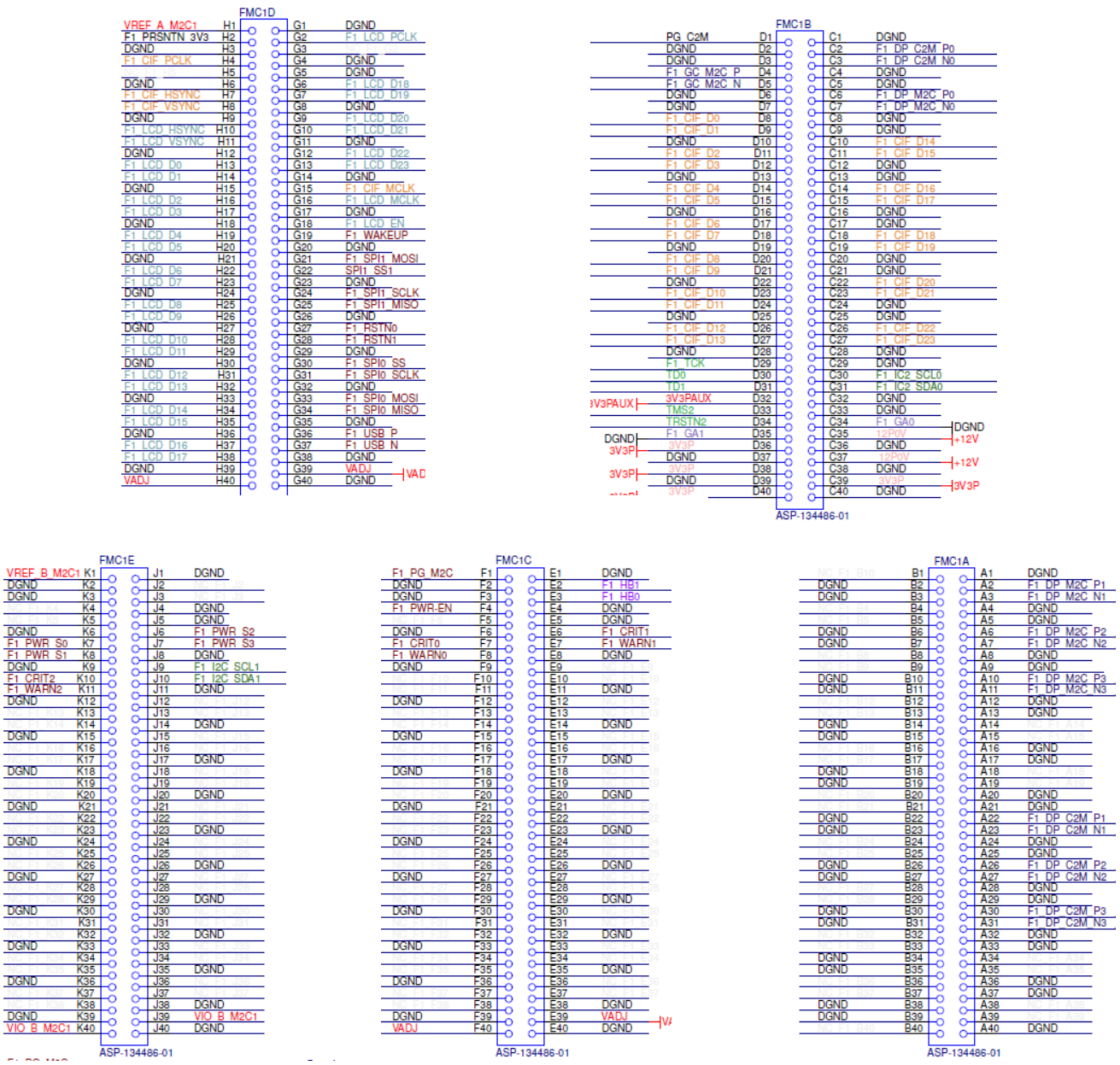

Figure 16 P1 FMC connector pinout

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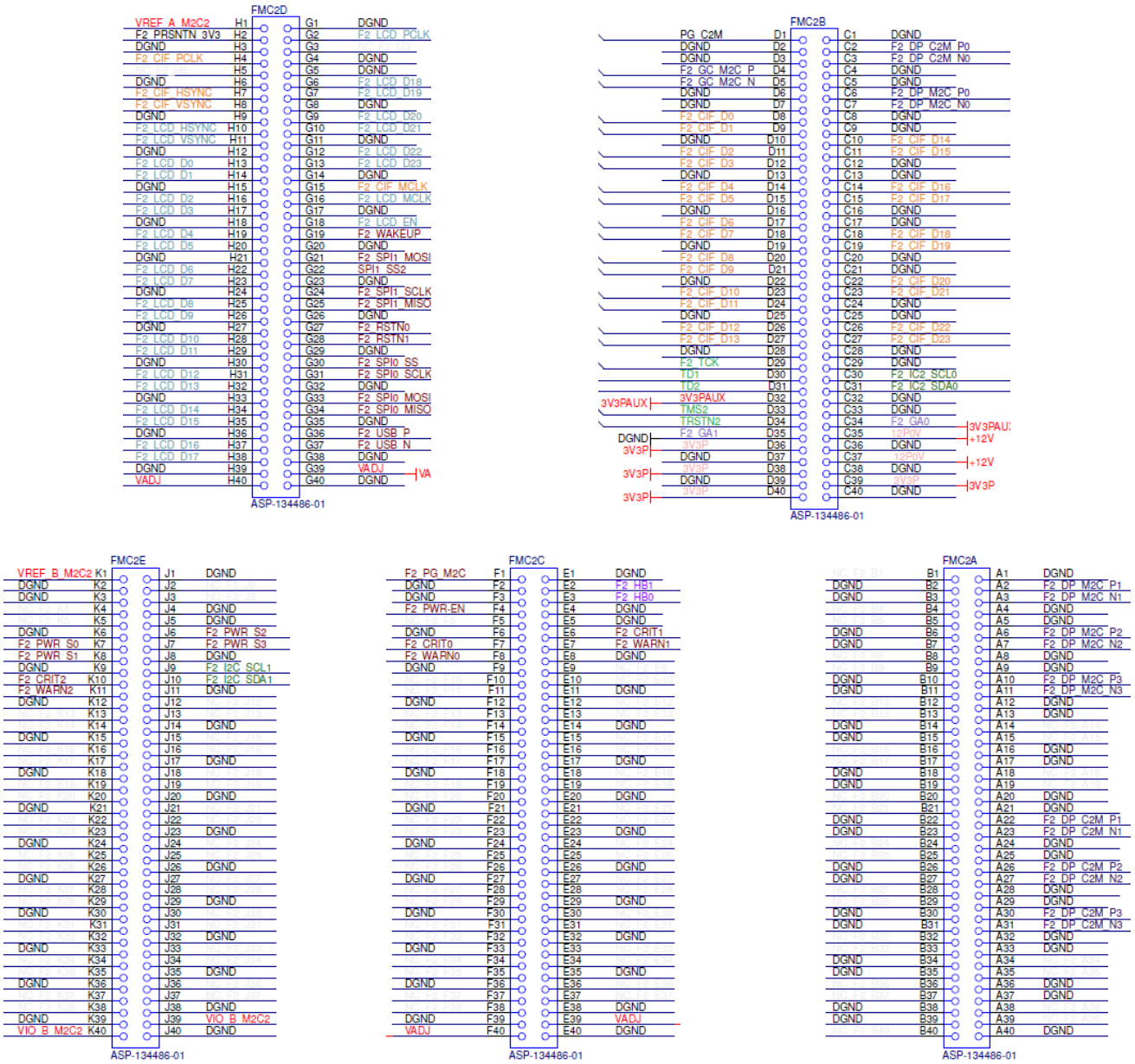

Figure 17 P2 FMC connector pinout

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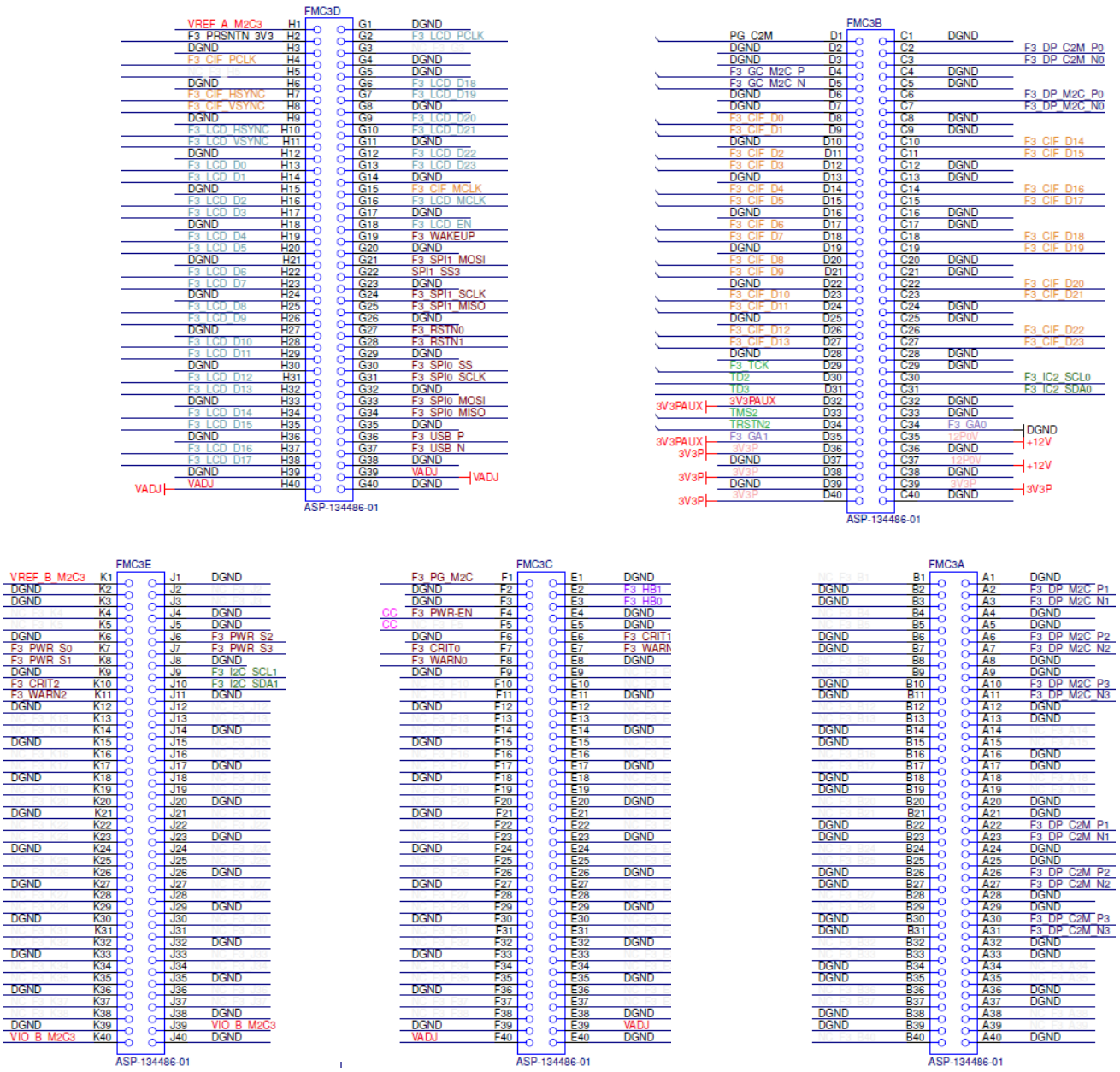

Figure 18 P3 FMC connector pinout

5.12.3 LCD

This is a data interface between the M2 and the FPGA on the Carrier Board comprising 29 signals:

LCD[23..0]

LCD_EN

LCD_MCLK

LCD_PCLK

LCD_HSYNC

LCD_VSYNC

These signals use 1.8V signalling logic.

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5.12.4 CIF

This is a data interface between the M2 and the FPGA on the main Carrier Board comprising 28 signals:

CIF[23..0]

CIF_MCLK

CIF_PCLK

CIF_HSYNC

CIF_VSYNC

These signals use 1.8V signalling logic.

5.12.5 SPI0

This 4 pin SPI interface connects to the GPIO interface pins of the M2.

This interface is understood to be used to load the boot program of the M2 with the FPGA on the Carrier Board as Master.

These signals use 1.8V signalling logic.

5.12.6 SPI1

This 4 pin SPI interface connects to the GPIO interface pins of the M2.

This interface is a signal/control interface with the GR716 on the Carrier Board as Master.

These signals on the M2 use 1.8V signalling logic. However, the SPI interface of the GR716 uses 3.3V signalling logic. Voltage conversion is therefore required on the Carrier Board.

5.12.7 SPI2

This 4 pin SPI interface connects to the GPIO interface pins of the M2.

This interface connects to a local SPI serial flash PROM.

This prom allows a local boot image to be stored in the SPI prom

The required size of this EEPROM has not be defined. A S25FL256 256 Mbit device in a WSON8 package has been implemented.

5.12.8 USB

See also section 5.11.

In order to reduce the number of interface signals and components required, only USB 2.0 is supported on this mezzanine interface.

These USB2 signals (DM, DP) connect via a 4-way USB hub on the Carrier Board to standard USB connector on the front panel.

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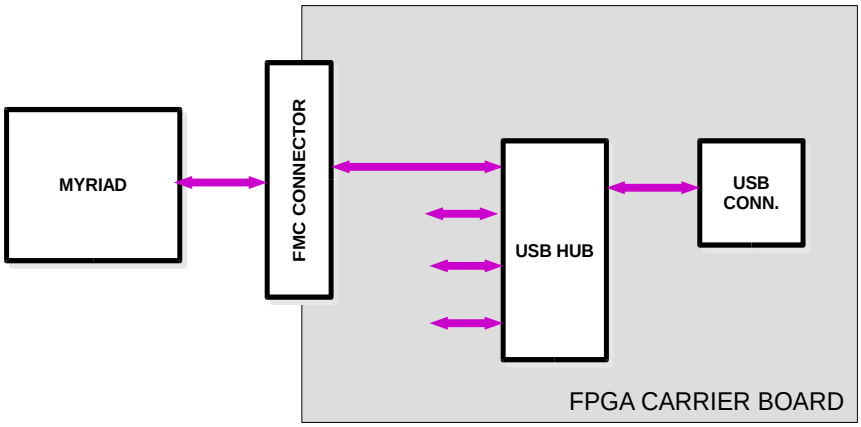

Figure 19 USB Interface

5.12.9 JTAG

The JTAG interface is connected to the FMC connector.

On the Carrier Board, multiple JTAG sources are daisy-chained and connected to an FTDI-USB interface to allow an external JTAG DSU connection to devices on the Mezzanine boards.

5.12.10 SYS-RSTN

A reset circuit is implemented on the Mezzanine board as shown in [RD8].

This circuit performs an 'or' of the following conditions and holds the M2 processor 'RESETN' input low if any of the conditions are low:

- PWR-GOOD (from power supply circuits)

- SYS-RSTN (from FMC connector)

- Push-Button S1 (on-board user reset)

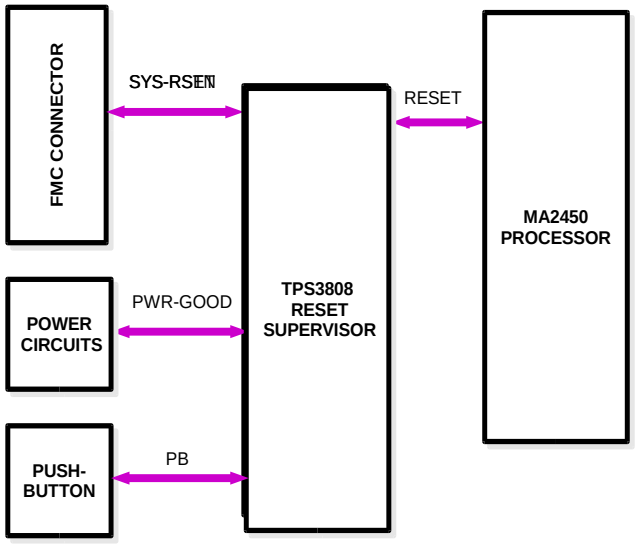

Figure 20 On-Board Reset Configuration

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5.12.11 WAKEUP

A 'Wake-up' input to the M2 processor is connected to the FMC connector.

This signal is connected to a dedicated pin of the M2 device (1.8V logic levels).

A pull-up to 1.8V and a miniature DIP switch to DGND are implemented on the FMC. The DIP switch S2 can be used to set the state of the pin. Alternatively, if this signal is to be driven from the Carrier Board, then the DIP switch should be 'open'.

5.12.12 HEARTBEAT[1..0]

Two signals are defined which provide a 'heartbeat' or 'alive' indicator from the Processors on the M2 device.

These signals pins are connected to GPIO pins of the M2 device (1.8V logic levels).

5.12.13 GA[1..0]

'Geographical Address' pins are defined in the FMC specification which allow a mezzanine board to identify which FMC slot it is plugged on to. These FMC connector pins are connected to GPIO pins of the M2 device. It may be necessary to use these pins in order that software running on the M2 can identify which to slot it is attached.

5.12.14 +12V

This is the main power input for the board.

For further information see [RD8].

5.12.15 ENABLEN

This is control signal from the Carrier Board which enables the power start up sequence of the converters on the FMC Mezzanine board to start.

The Logic Level of this signal is 1.8V to drive a logic FET which enables/disables start-up of the power sequencer.

PWR_EN is an Active Low signal which Starts and Stops the sequencer:

High => Transistor is ON, SEQ_EN is pulled low. Sequencer is stopped.

Low => Transistor is OFF, pull-up resistor pulls SEQ_EN high, Sequencer starts

NC => Transistor is OFF, pull-up resistor pulls SEQ_ EN high, Sequencer starts

5.12.16 PWR-GOOD

This signal is an 'or' of the 'Power Good' outputs of the various power converters and indicates whether the converters are operational.

For further information see [RD8].

5.12.17 S[3..0]

These signals are optional inputs to the board which could allow the FPGA on the Carrier Board to perform the power supply sequencing.

The Logic Level of these signals is 1.8V and will be driven from the FPGA on the Carrier Board. These signals have an 'active low' logic where:

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High => Transistor is ON, pull-up resistor pulls EN low

Low => Transistor is OFF, pull-up resistor pulls EN high

NC => Transistor is OFF, pull-up resistor pulls EN high

For further information see [RD8].

5.12.18 I2C

The VITA57.1 FMC standard requires that the mezzanine board includes a 2k I2C EEPROM that holds information about the Mezzanine board and its capabilities.

The data format and record contents are defined by the VITA57.1 standard.

This I2C interface is connected to the GR716 on the Carrier Board, and the GR716 must be able to read this PROM before the local power supplies have been enabled. This PROM must therefore be powered from the +3V3PAUX voltage on the FMC mezzanine connector.

In order to be program the I2C EEPROM a 4-pin header J3 is provided on the Mezzanine board.

5.13 VPX Backplane Interface

The overall connections to the VPX backplane are illustrated in the figure below.

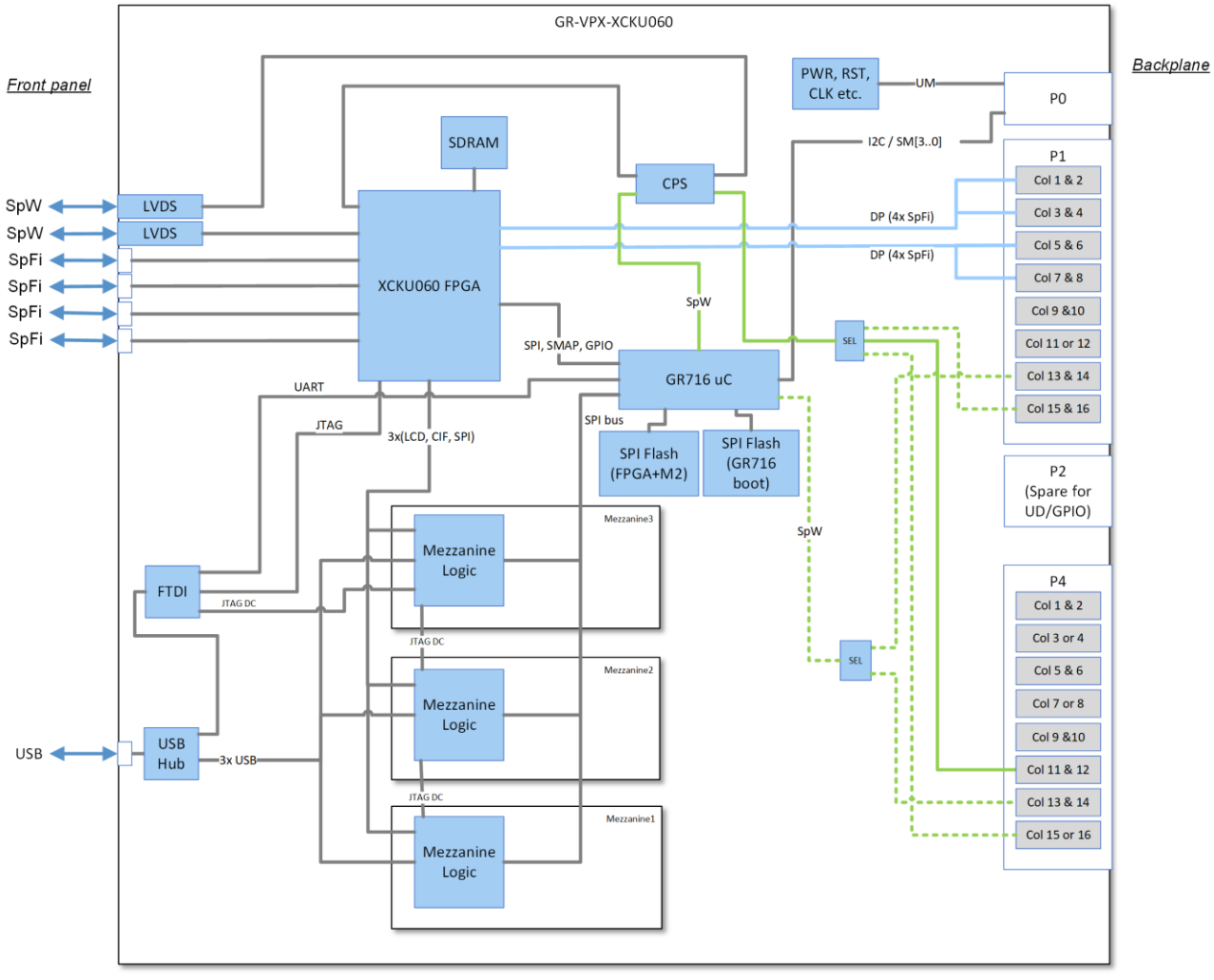

Figure 21 VPX backplane connections

The backplane connector is designed to comply with the OpenVPX (VITA 65) standard [RD4]), and specifically slot profile variant 10.2.1 intended for Payload modules. This slot profile is compatible with various OpenVPX backplane profiles, whereof variant 11.2.5 is one used for star configurations of control and data planes.

The compatibility to the slot profile above applies for default factory configuration of the *GR-VPX-XCKU* board, where SpaceWire routing is indicated as solid green lines in the figure above. The design also supports, if factory-configured, backplane connections to 6U and 3U backplane variants fulfilling the SpaceVPX (VITA 78) standard [RD5], payload slot profiles 10.2.1 and 14.2.3. These are indicated as green dashed lines in the figure.

The backplane connections include the following signals:

- SMBus connection to I2C Slave in *GR716* (2 pins)
- 4 x SpW links (each link 4 differential pairs = 8 pins)
  - 1 x DP-P1-nominal to SPW logic in FPGA
  - 1 x DP-P1-redundant to SPW logic in FPGA
  - 1 x CP-nominal to Cross-point switch
  - 1 x CP-redundant to SPW1 in GR716
- 4 x SPFI links (each link 2 differential pairs = 4 pins)
  - 2 x DP-nominal to GTH transceivers in FPGA
  - 2 x DP-redundant to GTH transceivers in FPGA
- DC supply

In the three tables below the pinouts for the connectors P0, P1 and P4 is specified in detail. Where the term “HPCB config” is referred, it defines the use as part of a 6U OpenVPX rack as described above.

Table 15 P0 connector pinout

Connector	Column	Attribute	Value	Signal	Use
P0	1	Row G	Vs1	VS1	Main +12V supply
P0	1	Row F	Vs1	VS1	Main +12V supply
P0	1	Row E	Vs1	VS1	Main +12V supply
P0	1	Row D	No Pad*	N.C.	
P0	1	Row C	Vs2	VS2	Secondary +12V supply possible
P0	1	Row B	Vs2	VS2	Secondary +12V supply possible
P0	1	Row A	Vs2	VS2	Secondary +12V supply possible
P0	2	Row G	Vs1	VS1	Main +12V supply
P0	2	Row F	Vs1	VS1	Main +12V supply
P0	2	Row E	Vs1	VS1	Main +12V supply
P0	2	Row D	No Pad*	N.C.	
P0	2	Row C	Vs2	VS2	Secondary +12V supply possible
P0	2	Row B	Vs2	VS2	Secondary +12V supply possible
P0	2	Row A	Vs2	VS2	Secondary +12V supply possible
P0	3	Row G	Vs3	+5V	Main +5V supply possible
P0	3	Row F	Vs3	+5V	Main +5V supply possible
P0	3	Row E	Vs3	+5V	Main +5V supply possible
P0	3	Row D	No Pad*	N.C.	
P0	3	Row C	Vs3	+5V	Main +5V supply possible
P0	3	Row B	Vs3	+5V	Main +5V supply possible
P0	3	Row A	Vs3	+5V	Main +5V supply possible
P0	4	Row G	SM2	SM2	GR716 I2C
P0	4	Row F	SM3	SM3	GR716 I2C
P0	4	Row E	GND	GND	

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Connector	Column	Attribute	Value	Signal	Use
P0	4	Row D	-12V_Aux	N.C.	Not used.
P0	4	Row C	GND	GND	
P0	4	Row B	SYSRESET*	SYSRESET_N	Input, route to reset logic.
P0	4	Row A	NVMRO	N.C.	Not used.
P0	5	Row G	GAP*	N.C.	Not used.
P0	5	Row F	GA4*	N.C.	Not used.
P0	5	Row E	GND	GND	
P0	5	Row D	3.3V_Aux	+3V3_AUX	Not used.
P0	5	Row C	GND	GND	
P0	5	Row B	SM0	SM0	GR716 I2C
P0	5	Row A	SM1	SM1	GR716 I2C
P0	6	Row G	GA3*	N.C.	Not used.
P0	6	Row F	GA2*	N.C.	Not used.
P0	6	Row E	GND	GND	
P0	6	Row D	+12V_Aux	N.C.	Not used.
P0	6	Row C	GND	GND	
P0	6	Row B	GA1*	N.C.	Not used.
P0	6	Row A	GA0*	N.C.	Not used.
P0	7	Row G	TCK	N.C.	Not used.
P0	7	Row F	GND	GND	
P0	7	Row E	TDO	N.C.	Not used.
P0	7	Row D	TDI	N.C.	Not used.
P0	7	Row C	GND	GND	
P0	7	Row B	TMS	N.C.	Not used.
P0	7	Row A	TRST*	N.C.	Not used.
P0	8	Row G	GND	GND	
P0	8	Row F	REF_CLK-	REF_CLK_IN_N	Route to FPGA I/O, 25MHz, input
P0	8	Row E	REF_CLK+	REF_CLK_IN_P	Route to FPGA I/O, 25MHz, input
P0	8	Row D	GND	GND	
P0	8	Row C	AUX_CLK-	AUX_CLK_IN_N	Route to FPGA I/O, 1 sec PPS, input
P0	8	Row B	AUX_CLK+	AUX_CLK_IN_P	Route to FPGA I/O, 1 sec PPS, input
P0	8	Row A	GND	GND	

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Table 16 P1 connector pinout

Connector	Column	Attribute	Value	Signal	Use
P1	1	Row G	GDiscrete1	SYS_CON_P	Not used.
P1	1	Row F	GND	GND	
P1	1	Row E	DP01-T0-	PL1N-SCR-DPL0-T-N	SpFi DP Lane 0: PL->Sys Controller Red
P1	1	Row D	DP01-T0+	PL1N-SCR-DPL0-T-P	SpFi DP Lane 0: PL->Sys Controller Red
P1	1	Row C	GND		
P1	1	Row B	DP01-R0-	SCR-PL1N-DPL0-R-N	SpFi DP Lane 0: Sys Controller Red->PL
P1	1	Row A	DP01-R0+	SCR-PL1N-DPL0-R-P	SpFi DP Lane 0: Sys Controller Red->PL
P1	2	Row G	GND		
P1	2	Row F	DP01-T1-	PL1N-SCR-DPL1-T-N	SpFi DP Lane 1: PL->Sys Controller Red
P1	2	Row E	DP01-T1+	PL1N-SCR-DPL1-T-P	SpFi DP Lane 1: PL->Sys Controller Red
P1	2	Row D	GND		
P1	2	Row C	DP15_T01R13_0_N	SCR-PL1N-DPL1-R-N	SpFi DP Lane 1: Sys Controller Red->PL
P1	2	Row B	DP01-R1+	SCR-PL1N-DPL1-R-P	SpFi DP Lane 1: Sys Controller Red->PL
P1	2	Row A	GND		
P1	3	Row G	P1-VBAT		
P1	3	Row F	GND		
P1	3	Row E	DP01-T2-	PL1N-SCR-DPL2-T-N	SpFi DP Lane 2: PL->Sys Controller Red
P1	3	Row D	DP01-T2+	PL1N-SCR-DPL2-T-P	SpFi DP Lane 2: PL->Sys Controller Red
P1	3	Row C	GND		
P1	3	Row B	DP01-R2-	SCR-PL1N-DPL2-R-N	SpFi DP Lane 2: Sys Controller Red->PL
P1	3	Row A	DP01-R2+	SCR-PL1N-DPL2-R-P	SpFi DP Lane 2: Sys Controller Red->PL
P1	4	Row G	GND		
P1	4	Row F	DP01-T3-	PL1N-SCR-DPL3-T-N	SpFi DP Lane 3: PL->Sys Controller Red
P1	4	Row E	DP01-T3+	PL1N-SCR-DPL3-T-P	SpFi DP Lane 3: PL->Sys Controller Red
P1	4	Row D	GND		
P1	4	Row C	DP01-R3-	SCR-PL1N-DPL3-R-N	SpFi DP Lane 3: Sys Controller Red->PL
P1	4	Row B	DP01-R3+	SCR-PL1N-DPL3-R-P	SpFi DP Lane 3: Sys Controller Red->PL
P1	4	Row A	GND		
P1	5	Row G	SYS_CON*	N.C.	Not used.
P1	5	Row F	GND		
P1	5	Row E	DP02-T0-	PL1N-SCN-DPL0-T-N	SpFi Lane 0: PL1N->EBB
P1	5	Row D	DP02-T0+	PL1N-SCN-DPL0-T-P	SpFi Lane 0: PL1N->EBB
P1	5	Row C	GND		
P1	5	Row B	DP02-R0-	SCN-PL1N-DPL0-R-N	SpFi Lane 0: EBB->PL1N
P1	5	Row A	DP02-R0+	SCN-PL1N-DPL0-R-P	SpFi Lane 0: EBB->PL1N
P1	6	Row G	GND		
P1	6	Row F	DP02-T1-	PL1N-SCN-DPL1-T-N	SpFi Lane 1: PL1N->EBB
P1	6	Row E	DP02-T1+	PL1N-SCN-DPL1-T-P	SpFi Lane 1: PL1N->EBB
P1	6	Row D	GND		
P1	6	Row C	DP02-R1-	SCN-PL1N-DPL1-R-N	SpFi Lane 1: EBB->PL1N
P1	6	Row B	DP02-R1+	SCN-PL1N-DPL1-R-P	SpFi Lane 1: EBB->PL1N
P1	6	Row A	GND		
P1	7	Row G	Reserved		
P1	7	Row F	GND		
P1	7	Row E	DP02-T2-	PL1N-SCN-DPL2-T-N	SpFi Lane 2: PL1N->EBB
P1	7	Row D	DP02-T2+	PL1N-SCN-DPL2-T-P	SpFi Lane 2: PL1N->EBB
P1	7	Row C	GND		
P1	7	Row B	DP02-R2-	SCN-PL1N-DPL2-R-N	SpFi Lane 2: EBB->PL1N
P1	7	Row A	DP02-R2+	SCN-PL1N-DPL2-R-P	SpFi Lane 2: EBB->PL1N
P1	8	Row G	GND		
P1	8	Row F	DP02-T3-	PL1N-SCN-DPL3-T-N	SpFi Lane 3: PL1N->EBB
P1	8	Row E	DP02-T3+	PL1N-SCN-DPL3-T-P	SpFi Lane 3: PL1N->EBB
P1	8	Row D	GND		
P1	8	Row C	DP02-R3-	SCN-PL1N-DPL3-R-N	SpFi Lane 3: EBB->PL1N
P1	8	Row B	DP02-R3+	SCN-PL1N-DPL3-R-P	SpFi Lane 3: EBB->PL1N
P1	8	Row A	GND		
P1	9	Row G	UD		
P1	9	Row F	GND		
P1	9	Row E	DP03-T0-	N.C.	
P1	9	Row D	DP03-T0+	N.C.	
P1	9	Row C	GND		
P1	9	Row B	DP03-R0-	N.C.	
P1	9	Row A	DP03-R0+	N.C.	
P1	10	Row G	GND		
P1	10	Row F	DP03-T1-	N.C.	

Connector	Column	Attribute	Value	Signal	Use
P1	10	Row E	DP03-T1+	N.C.	
P1	10	Row D	GND		
P1	10	Row C	DP03-R1-	N.C.	
P1	10	Row B	DP03-R1+	N.C.	
P1	10	Row A	GND		
P1	11	Row G	UD		
P1	11	Row F	GND		
P1	11	Row E	DP03-T2-	N.C.	
P1	11	Row D	DP03-T2+	N.C.	
P1	11	Row C	GND		
P1	11	Row B	DP03-R2-	N.C.	
P1	11	Row A	DP03-R2+	N.C.	
P1	12	Row G	GND		
P1	12	Row F	DP03-T3-	N.C.	
P1	12	Row E	DP03-T3+	N.C.	
P1	12	Row D	GND		
P1	12	Row C	DP03-R3-	N.C.	
P1	12	Row B	DP03-R3+	N.C.	
P1	12	Row A	GND		
P1	13	Row G	UD		
P1	13	Row F	GND		
P1	13	Row E	DP04-T0-	<See "Use" col>	Connect to switch. HPCB config: N.C. V78 3U config: SpW SCR, signal CPr_SpW_3U_SV
P1	13	Row D	DP04-T0+	-"-	-"-
P1	13	Row C	GND		
P1	13	Row B	DP04-R0-	-"-	-"-
P1	13	Row A	DP04-R0+	-"-	-"-
P1	14	Row G	GND		
P1	14	Row F	DP04-T1-	-"-	-"-
P1	14	Row E	DP04-T1+	-"-	-"-
P1	14	Row D	GND		
P1	14	Row C	DP04-R1-	-"-	-"-
P1	14	Row B	DP04-R1+	-"-	-"-
P1	14	Row A	GND		
P1	15	Row G	Maskable Reset*		Not used.
P1	15	Row F	GND		
P1	15	Row E	DP04-T2-	<See "Use" col>	Connect to switch. HPCB config: N.C. V78 3U config: SpW SCN, signal CPn_SpW_3U_SV
P1	15	Row D	DP04-T2+	-"-	-"-
P1	15	Row C	GND		
P1	15	Row B	DP04-R2-	-"-	-"-
P1	15	Row A	DP04-R2+	-"-	-"-
P1	16	Row G	GND		
P1	16	Row F	DP04-T3-	-"-	-"-
P1	16	Row E	DP04-T3+	-"-	-"-
P1	16	Row D	GND		
P1	16	Row C	DP04-R3-	-"-	-"-
P1	16	Row B	DP04-R3+	-"-	-"-
P1	16	Row A	GND		

Table 17 P4 connector pinout

Connector	Column	Attribute	Value	Signal	Use
P4	1	Row G	UD		
P4	1	Row F	GND		
P4	1	Row E	UD		
P4	1	Row D	UD		
P4	1	Row C	GND		
P4	1	Row B	UD		
P4	1	Row A	UD		
P4	2	Row G	GND		
P4	2	Row F	UD		
P4	2	Row E	UD		
P4	2	Row D	GND		
P4	2	Row C	UD		
P4	2	Row B	UD		
P4	2	Row A	GND		
P4	3	Row G	UD		
P4	3	Row F	GND		
P4	3	Row E	UD		
P4	3	Row D	UD		
P4	3	Row C	GND		
P4	3	Row B	UD		
P4	3	Row A	UD		
P4	4	Row G	GND		
P4	4	Row F	UD		
P4	4	Row E	UD		
P4	4	Row D	GND		
P4	4	Row C	UD		
P4	4	Row B	UD		
P4	4	Row A	GND		
P4	5	Row G	UD		
P4	5	Row F	GND		
P4	5	Row E	UD		
P4	5	Row D	UD		
P4	5	Row C	GND		
P4	5	Row B	UD		
P4	5	Row A	UD		
P4	6	Row G	GND		
P4	6	Row F	UD		
P4	6	Row E	UD		
P4	6	Row D	GND		
P4	6	Row C	UD		
P4	6	Row B	UD		
P4	6	Row A	GND		
P4	7	Row G	UD		
P4	7	Row F	GND		
P4	7	Row E	UD		
P4	7	Row D	UD		
P4	7	Row C	GND		
P4	7	Row B	UD		
P4	7	Row A	UD		
P4	8	Row G	GND		
P4	8	Row F	UD		
P4	8	Row E	UD		
P4	8	Row D	GND		
P4	8	Row C	UD		
P4	8	Row B	UD		
P4	8	Row A	GND		
P4	9	Row G	UD		
P4	9	Row F	GND		
P4	9	Row E	UD		
P4	9	Row D	UD		
P4	9	Row C	GND		
P4	9	Row B	UD		
P4	9	Row A	UD		
P4	10	Row G	GND		
P4	10	Row F	UD		

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Connector	Column	Attribute	Value	Signal	Use
P4	10	Row E	UD		
P4	10	Row D	GND		
P4	10	Row C	UD		
P4	10	Row B	UD		
P4	10	Row A	GND		
P4	11	Row G	UD		
P4	11	Row F	GND		
P4	11	Row E	CPutp02-T-	PL1N-SCN-CP-6UOV-S-N	Connect to switch. HPCB config: OpenVPX 6U config: SpW SCN, signal CPn_SpW_6U_OV
P4	11	Row D	CPutp02-T+	PL1N-SCN-CP-6UOV-S-P	-"-
P4	11	Row C	GND		
P4	11	Row B	CPutp02-R-	SCN-PL1N-CP-6UOV-S-N	-"-
P4	11	Row A	CPutp02-R+	SCN-PL1N-CP-6UOV-S-P	-"-
P4	12	Row G	GND		
P4	12	Row F	CPutp01-T-	PL1N-SCN-CP-6UOV-D-N	-"-
P4	12	Row E	CPutp01-T+	PL1N-SCN-CP-6UOV-D-P	-"-
P4	12	Row D	GND		
P4	12	Row C	CPutp01-R-	SCN-PL1N-CP-6UOV-D-N	-"-
P4	12	Row B	CPutp01-R+	SCN-PL1N-CP-6UOV-D-P	-"-
P4	12	Row A	GND		
P4	13	Row G	UD		
P4	13	Row F	GND		
P4	13	Row E	CPtp02-DB-	<See "Use" col>	Connecto to switch. HPCB config: N.C. V78 config: SpW for CP: SCr<->PL
P4	13	Row D	CPtp02-DB+	-"-	-"-
P4	13	Row C	GND		
P4	13	Row B	CPtp02-DA-	-"-	-"-
P4	13	Row A	CPtp02-DA+	-"-	-"-
P4	14	Row G	GND		
P4	14	Row F	CPtp02-DD-	-"-	-"-
P4	14	Row E	CPtp02-DD+	-"-	-"-
P4	14	Row D	GND		
P4	14	Row C	CPtp02-DC-	-"-	-"-
P4	14	Row B	CPtp02-DC+	-"-	-"-
P4	14	Row A	GND		
P4	15	Row G	UD		
P4	15	Row F	GND		
P4	15	Row E	CPtp01-DB-	<See "Use" col>	Connecto to switch. HPCB config: N.C. V78 config: SpW for CP: SCn<->PL
P4	15	Row D	CPtp01-DB+	-"-	-"-
P4	15	Row C	GND		
P4	15	Row B	CPtp01-DA-	-"-	-"-
P4	15	Row A	CPtp01-DA+	-"-	-"-
P4	16	Row G	GND		
P4	16	Row F	CPtp01-DD-	-"-	-"-
P4	16	Row E	CPtp01-DD+	-"-	-"-
P4	16	Row D	GND		
P4	16	Row C	CPtp01-DC-	-"-	-"-
P4	16	Row B	CPtp01-DC+	-"-	-"-
P4	16	Row A	GND		

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5.14 Power

Power is nominally provided via the VPX backplane. In stand-alone operation, external DC supply can also be provided via header J12.

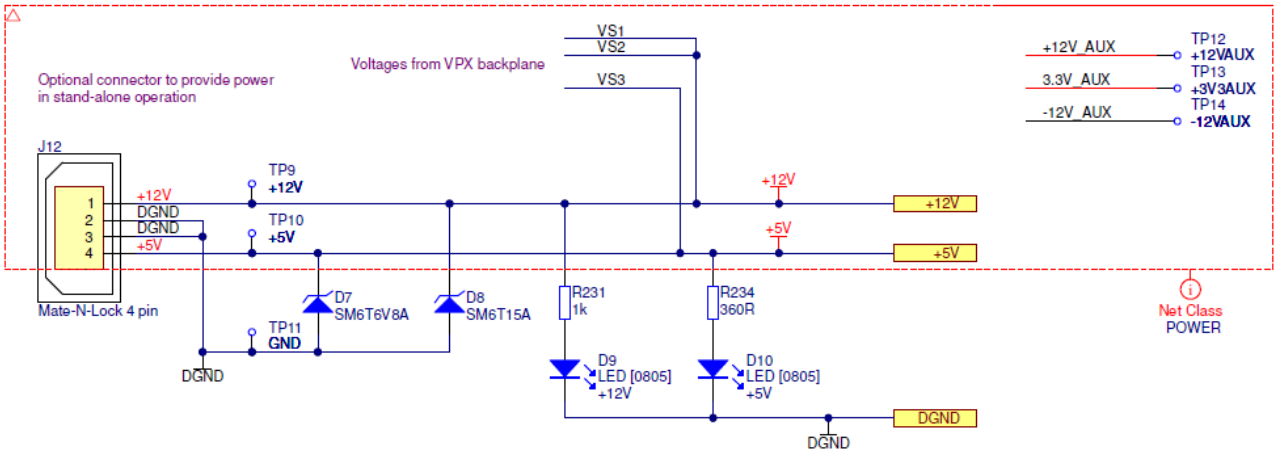

Figure 22 DC supply options

5.15 Headers

5.15.1 J11 – FPGA JTAG

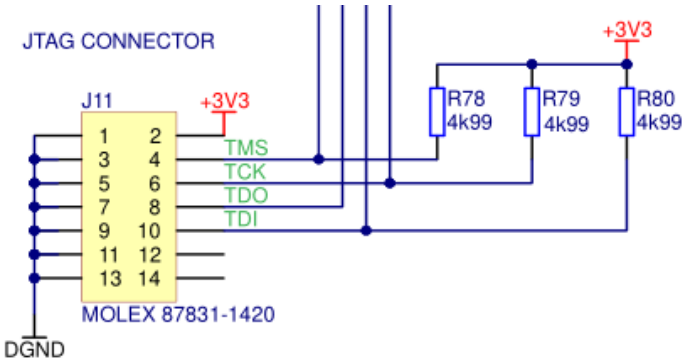

Figure 23 Pinout for the FPGA JTAG header.

When this header is used, JP5 should be open to disconnect the FTDI-USB device (see section 5.16.5).

5.15.2 J12 - Power

See section 5.14 above.

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5.15.3 J13 - Optional SM-bus

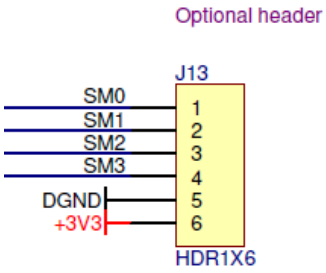


Figure 24 SM-bus header

5.15.4 J14 - Optional FPGA fan

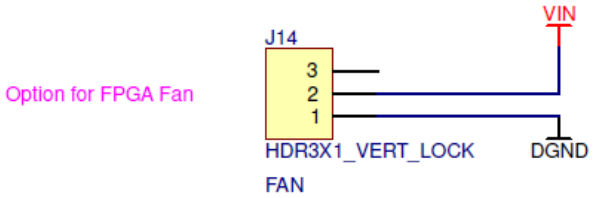


Figure 25 FPGA fan header

5.15.5 J15 - Optional PM bus

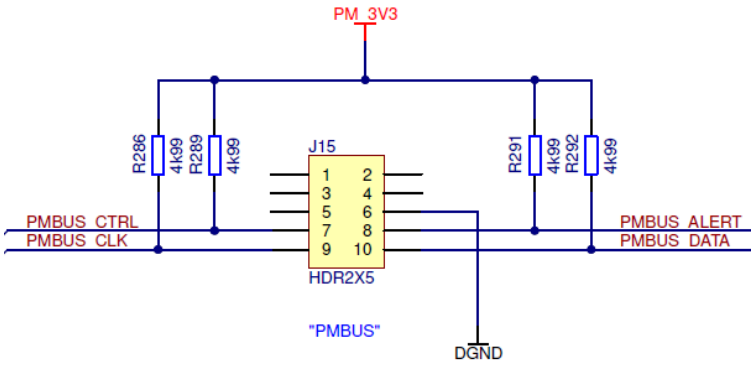
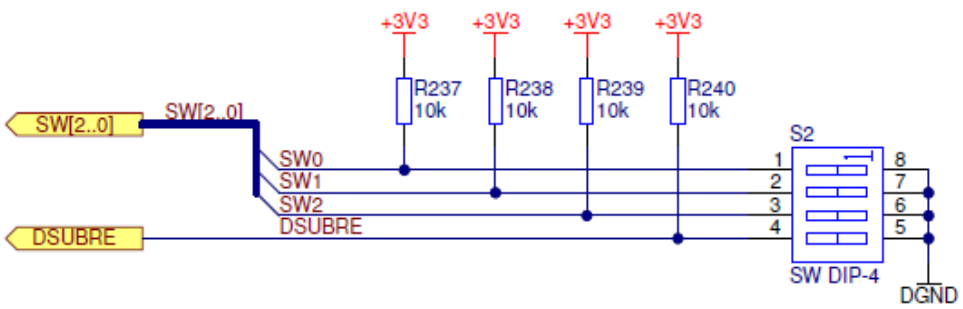


Figure 26 PM bus header

5.16 Switches and buttons

5.16.1 S2 - DIP Switch

The is a 4-pole DIP switch used to control GR716 DSU-Break and FPGA control signals USR[2..0]).



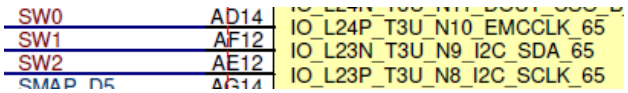


Figure 27 GR716 and FPGA configuration

5.16.2 JP1 - SelectMAP

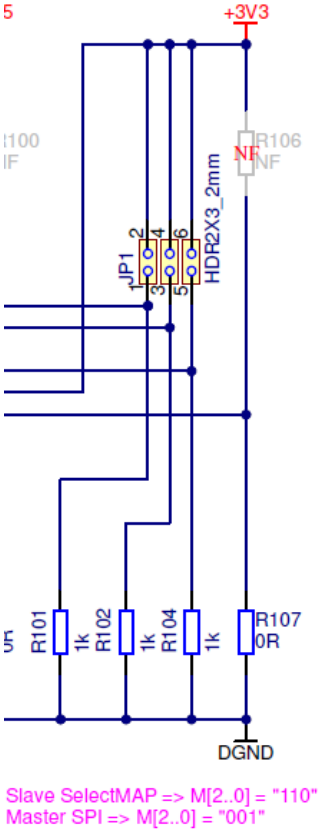


Figure 28 SelectMAP setting

5.16.3 JP2 - FPGA spare

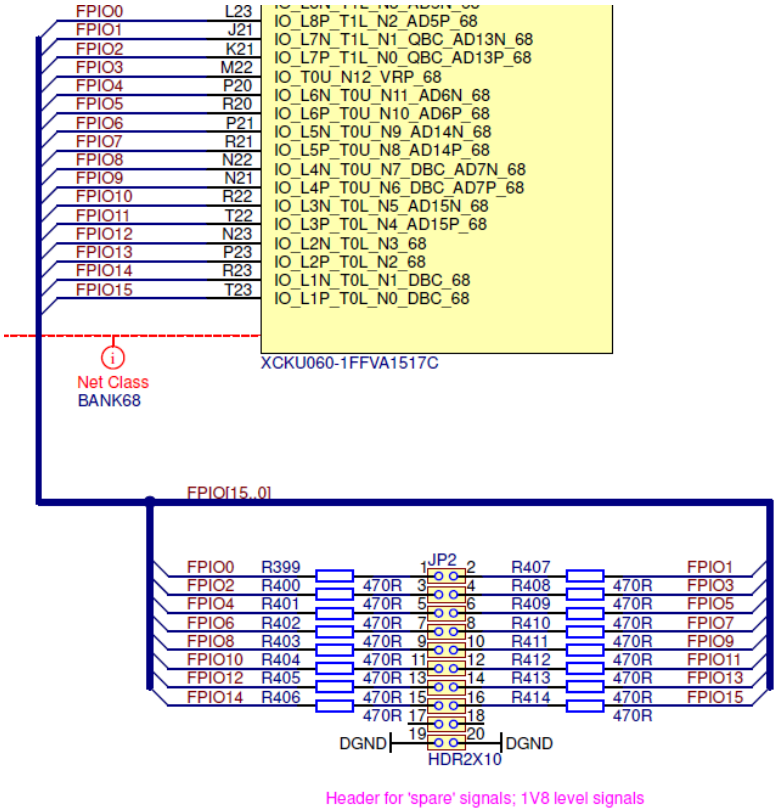


Figure 29 FPGA spare signal setting

5.16.4 JP3 - SpW cross-point switch settings

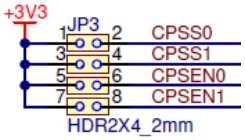


Figure 30 SpW cross-point switch setting

Configuration 1: GR716 connects to backplane, FPGA connects to front-panel

- S0 open
- S1 closed
- EN0 closed
- EN 1 closed

Configuration 2: GR716 connects to front panel, FPGA connects to backplane

- S0 closed
- S1 open
- EN0 closed
- EN1 closed

Configuration 3: GR716 connects to front panel, backplane link disabled

S0 don’t care

- S1 open
- EN0 open
- EN1 closed

5.16.5 JP4-JP6 - UART and JTAG access

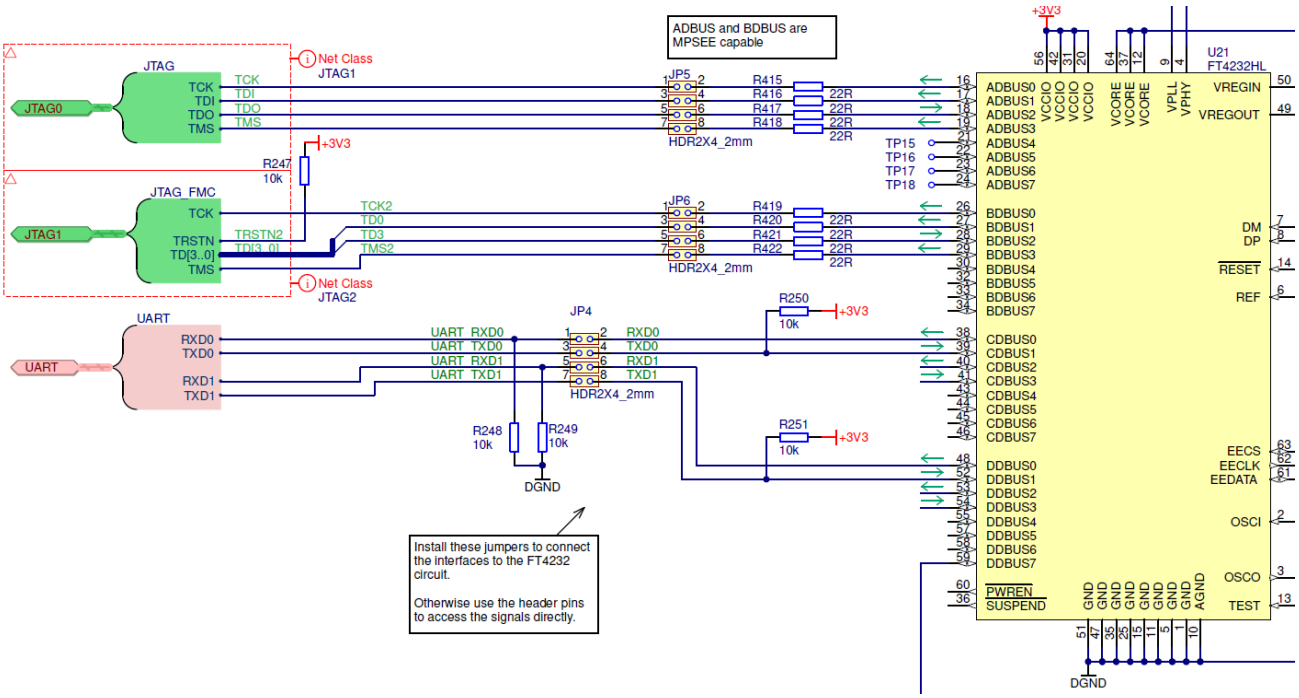


Figure 31 SpW cross-point switch setting

5.17 LEDs

Detailed information for some LED functions follows below.

5.17.1 D6 - FPGA initiation

5.17.2 D11 – VIN

5.17.3 D12 - PG_C2M

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6 MECHANICAL DESCRIPTION

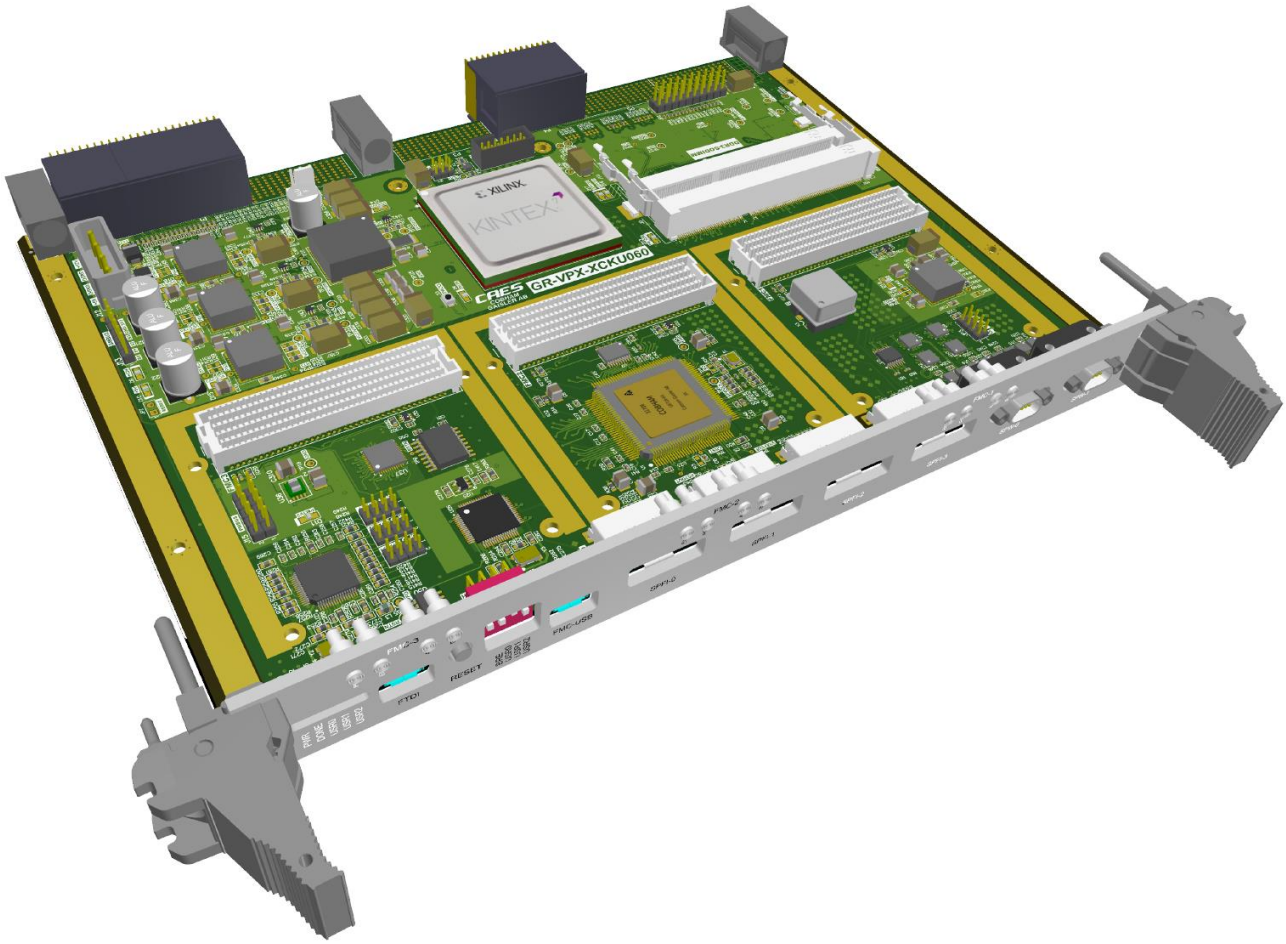

Figure 32 Top view

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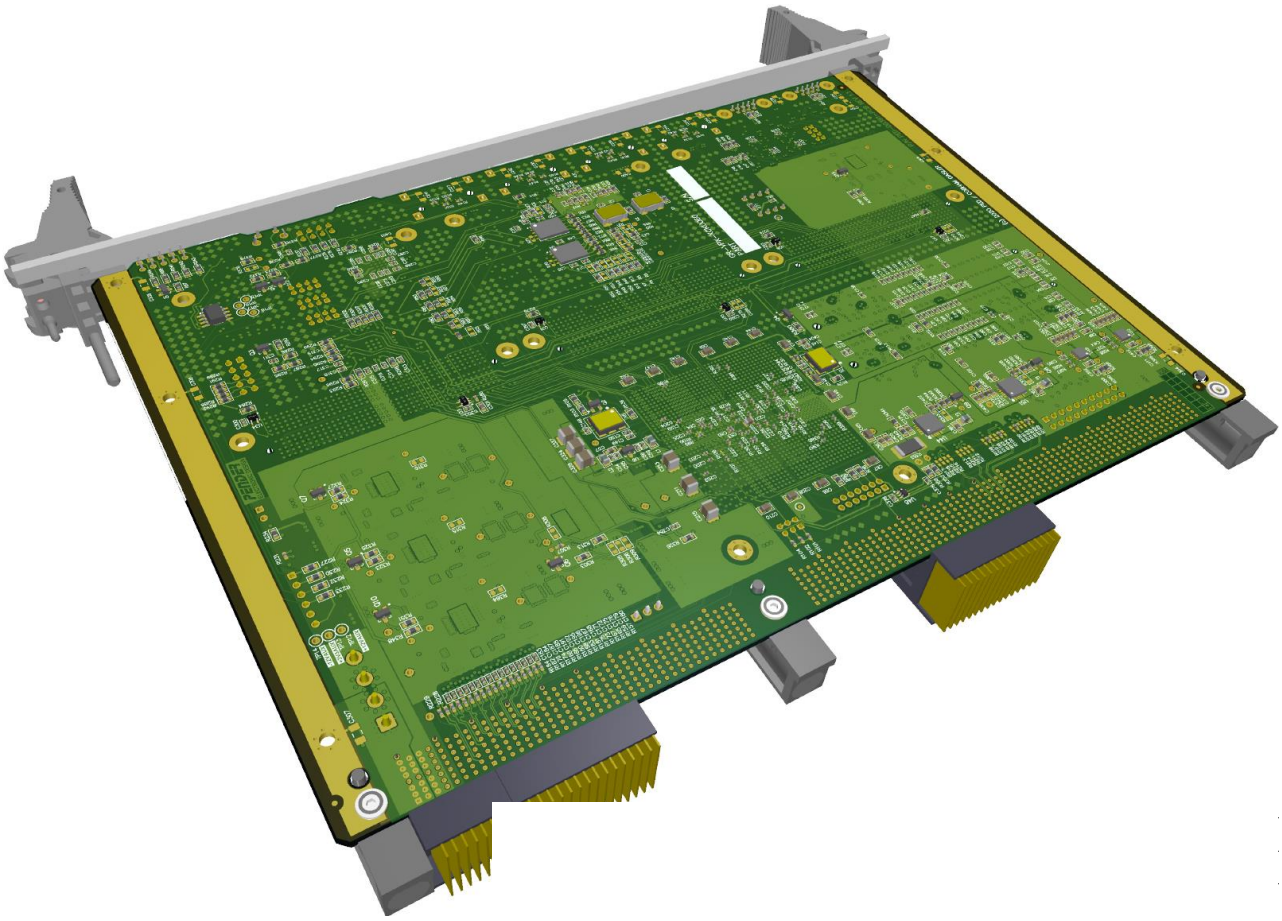

Figure 33 Top view

The design implemented is a 6U high, 1 slot (25.4mm) wide module for mounting in the controller slot of a 6U rack with a VPX Backplane. The dimensions of the main PCB are therefore 233.35x160mm (excluding the connector protrusions).

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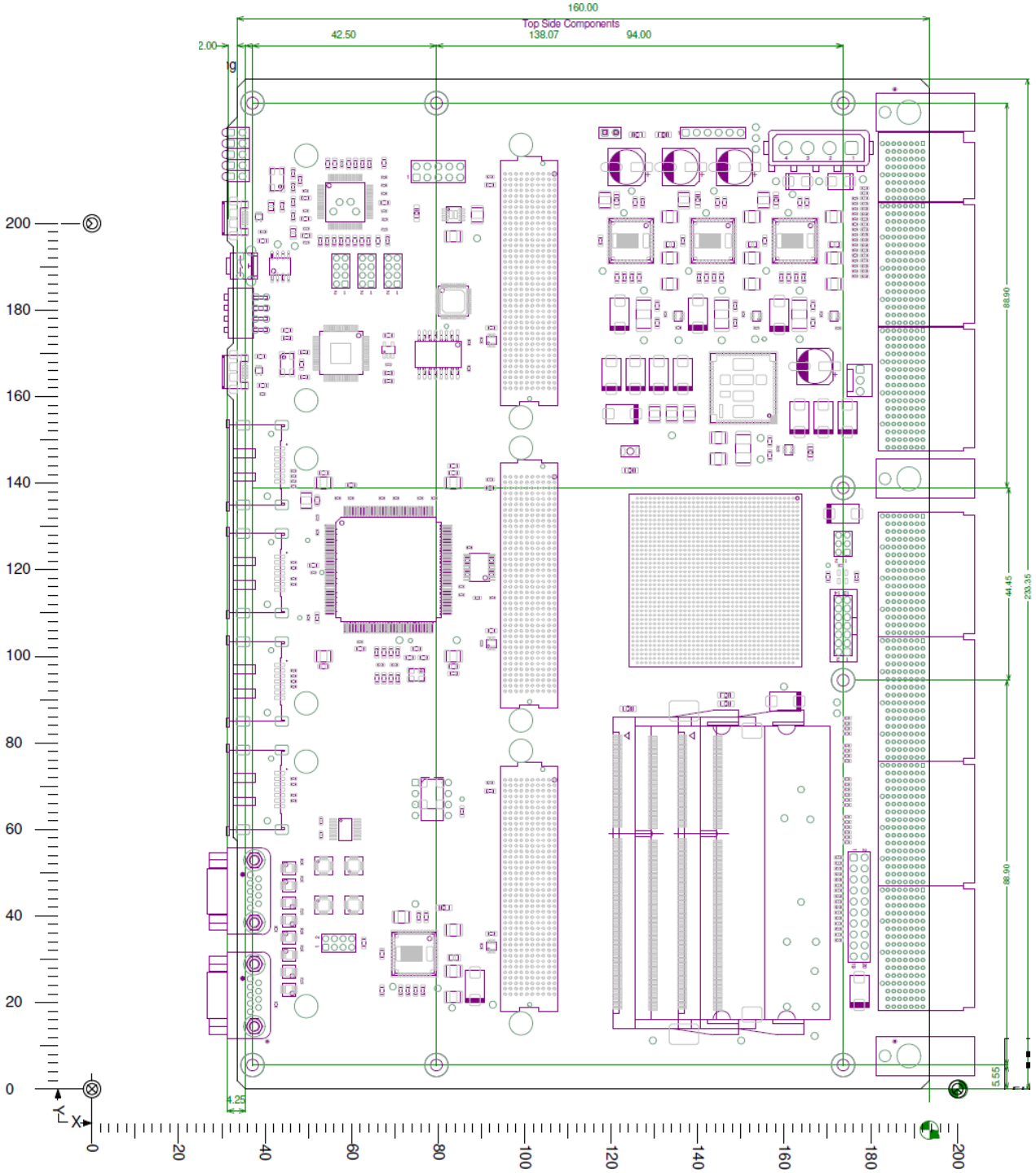

Figure 34 Board dimensions

The front panel provides access to the following interfaces, described in detail in section 5.2:

- 2 x MDM9S connectors for SPW interfaces
- 4 x E-SATA connectors for SPFI interfaces
- Mini/Micro USB connector for USB hub interface to FMC boards
- Mini/Micro USB connector for FTDI interface (JTAG0/1 and UART0/1)
- Push button switch (S1: RESET)

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- 4-pole DIP switch (S2: GR716 DSU-Break, FPGA_USR[2..0])
- 5 x LED indicators (POWER, DONE, USR0, USR1, USR2)
- 12 x LED indicators reserved for *GR-HPCB-FMC-M2* boards

A custom front panel with suitable cut-outs and markings is required. The figure below, represents the front panel (PED-00383-DWG) which is specifically designed for use with three *GR-HPCB-FMC-M2* FMC boards installed (not required).

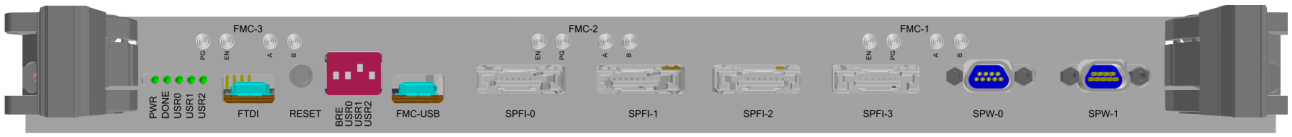

Figure 35 6U front panel layout

The figure below illustrates a setup with three *GR-HPCB-FMC-M2* boards installed.

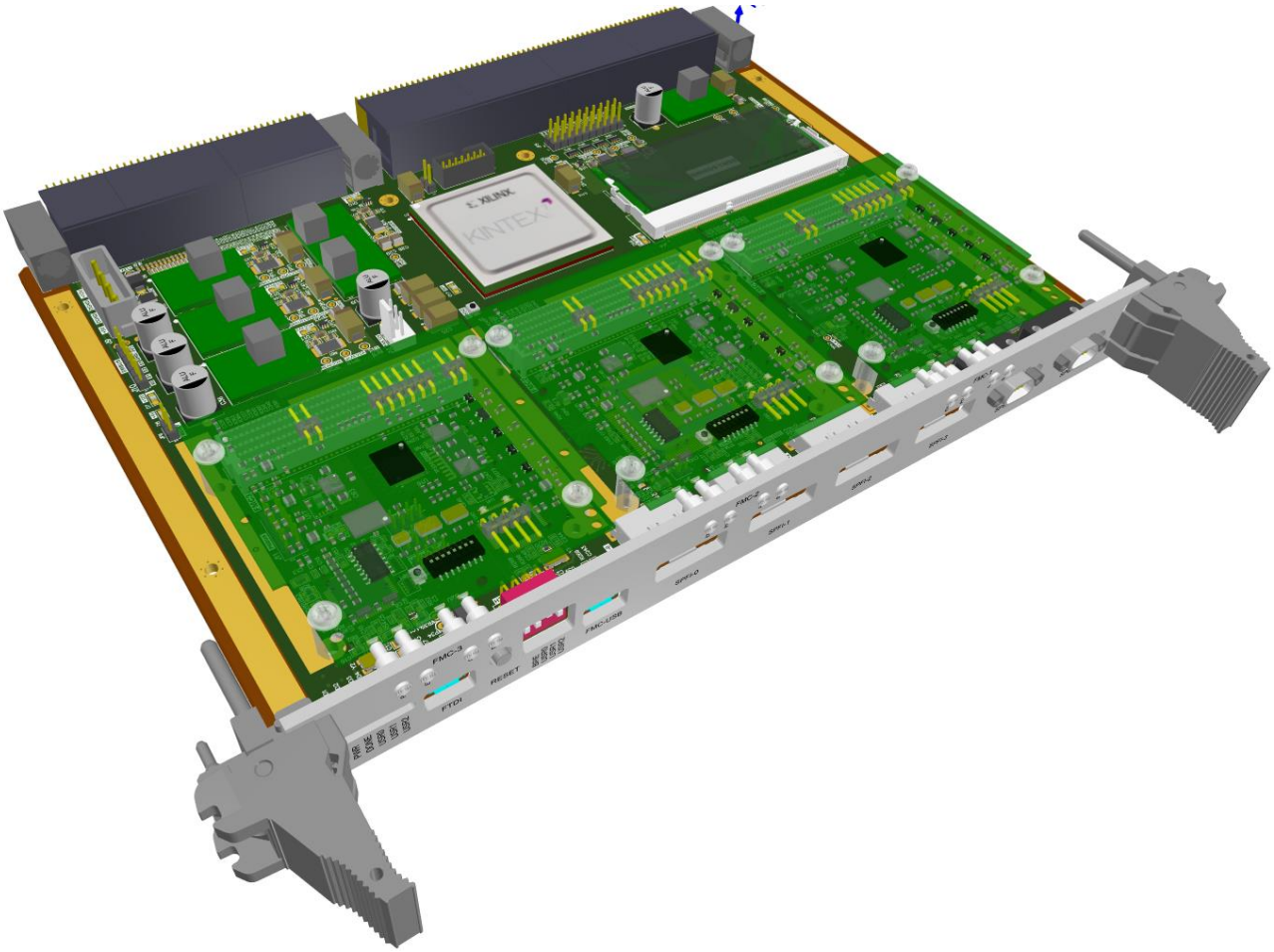

Figure 36 GR-VPX-XCKU060 Module concept

Kungsgatan 12 | SE-411 19 Goteborg | Sweden
+46 31 7758650 | www.caes.com/gaisler

Cobham Gaisler AB
Kungsgatan 12
411 19 Göteborg
Sweden
www.caes.com/gaisler
sales@gaisler.com
T: +46 31 7758650